Innovative, Versatile and Cost-Effective Solid Oxide Fuel Cell Stack Concept

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Innovative, Versatile and Cost-Effective SOFC Stack Concept Project

- Project: Innovative, Versatile and Cost-Effective Solid Oxide Fuel Cell Stack Concept (DE-FE0026211)

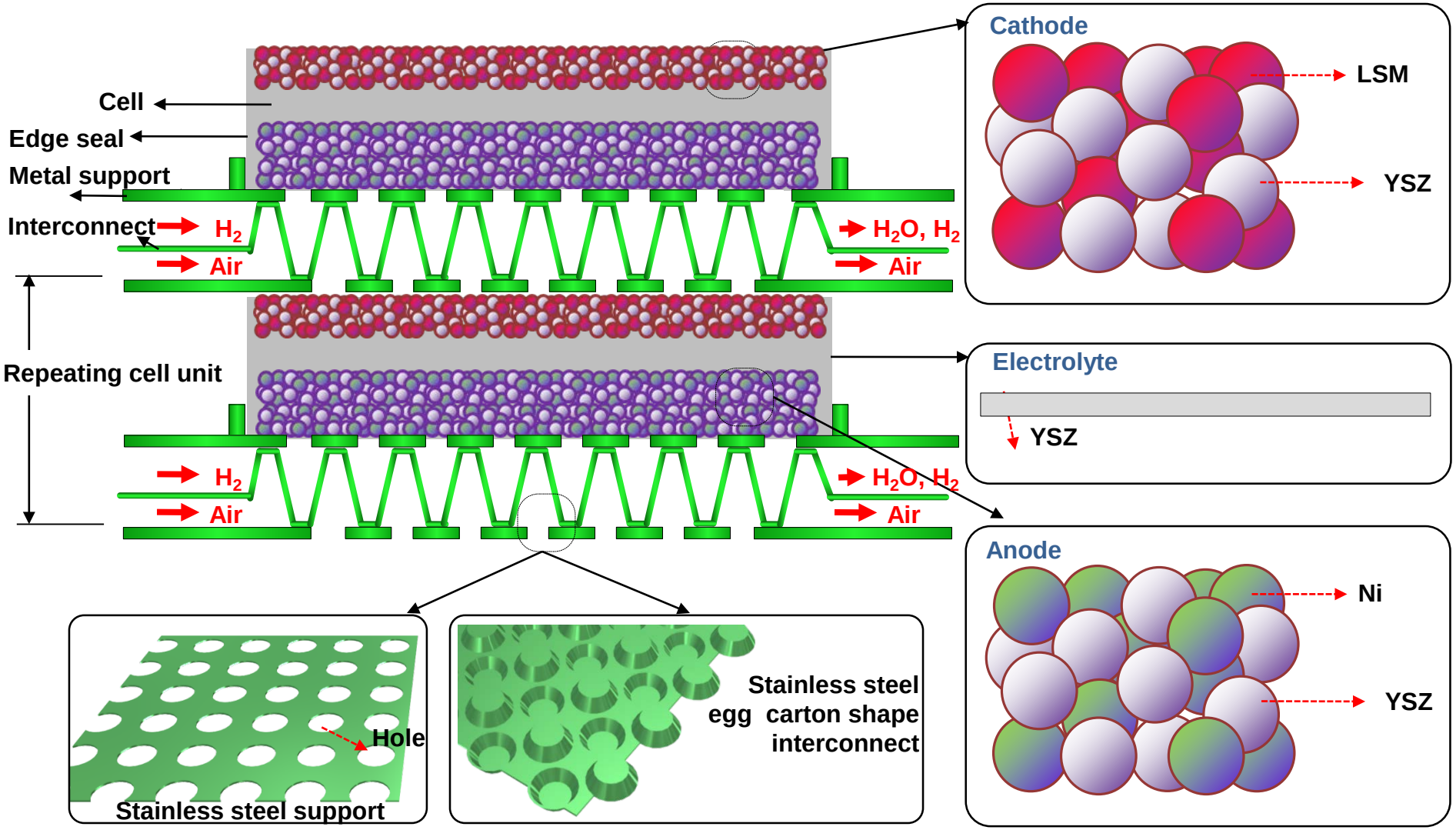
- Project Objective: Develop and evaluate a versatile stack configuration based on a prime-surface interconnect design that can incorporate different types of cell construction for a broad range of power generation applications

- DOE/NETL Project Manager: Dr. Patcharin Burke

- UCSD Project Team:
    - *Center for Energy Research*: Dr. Nguyen Minh (PI), Dr. Yoon Ho Lee (Postdoctoral scholar), Dr. Tuyen Tran (Visiting scholar)
    - *Department of Electrical Engineering and Center for Memory and Recording Research*: Dr. Eric Fullerton, Haowen Ren (graduate student)
    - *Department of NanoEngineering*: Dr. Shirley Meng, Erik Wu (graduate student

Stack Design

Incorporating Conventional Cells

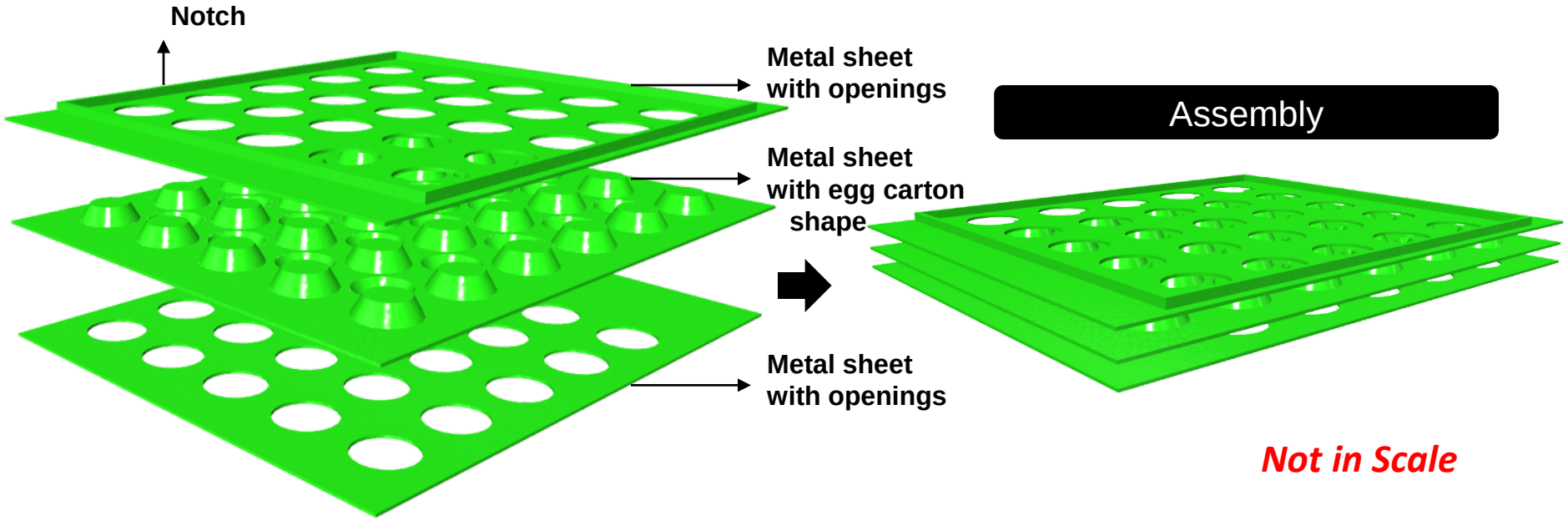


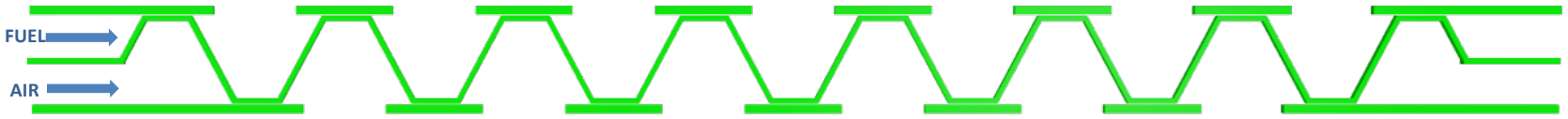
Features of Stack Concept

- Reduced weight and volume
- Flexibility in gas flow configuration
- Reduced stacking performance losses
- Improved sealing
- Versatility in incorporation of different types of cell construction

STACK DESIGN CONCEPT

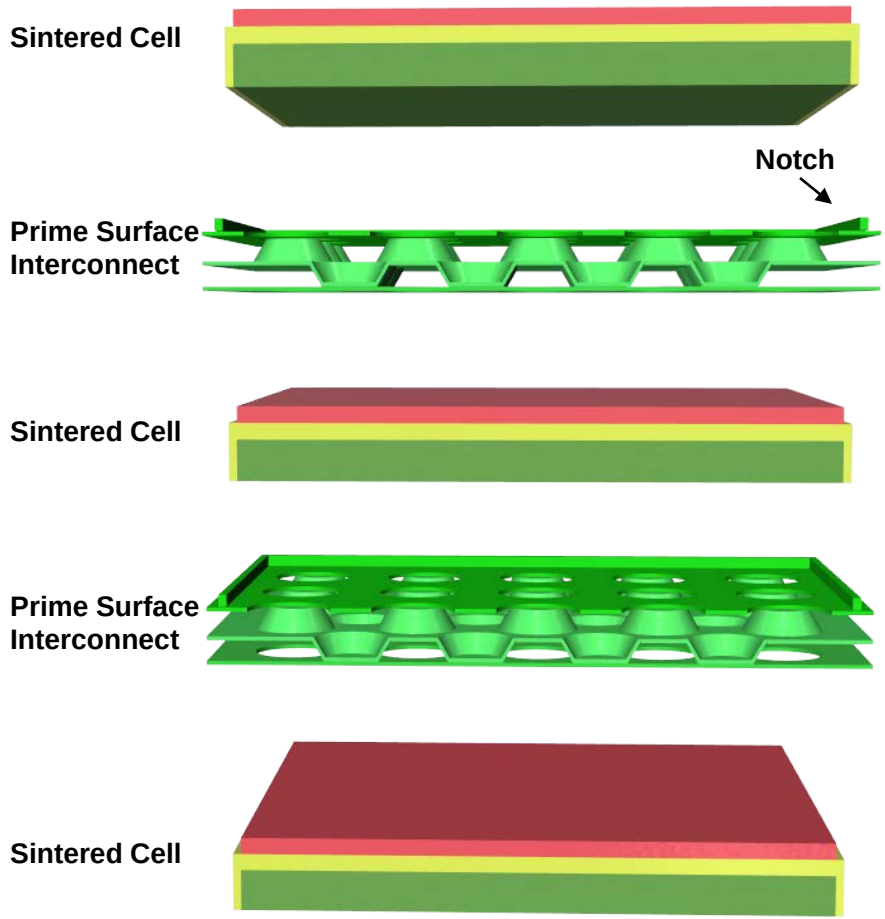
Prime-Surface Interconnect Design

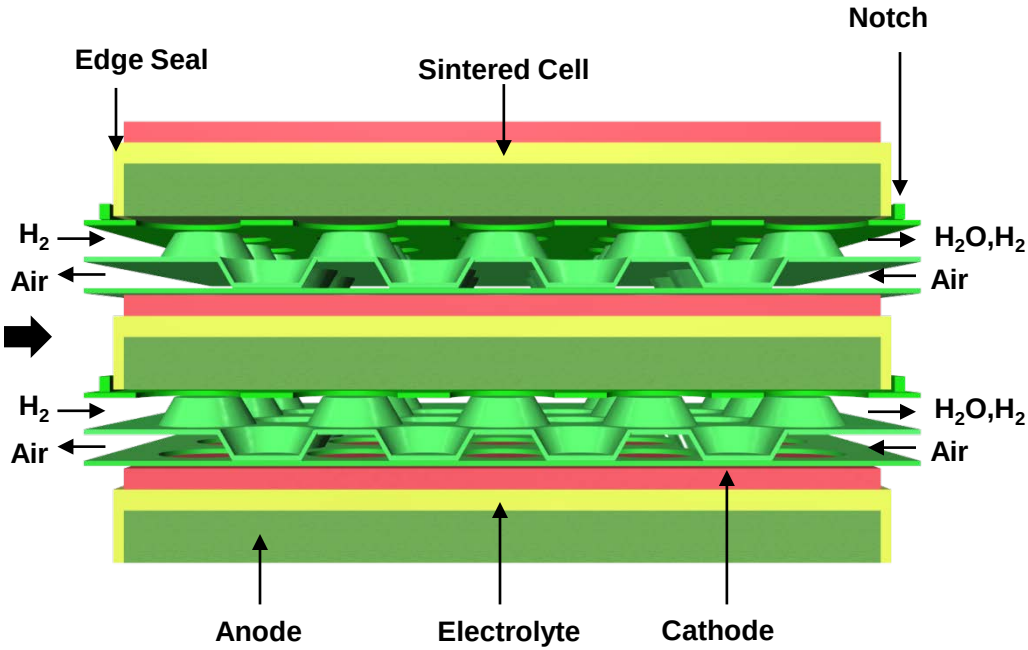




Stack Design

Incorporating Sintered Cells

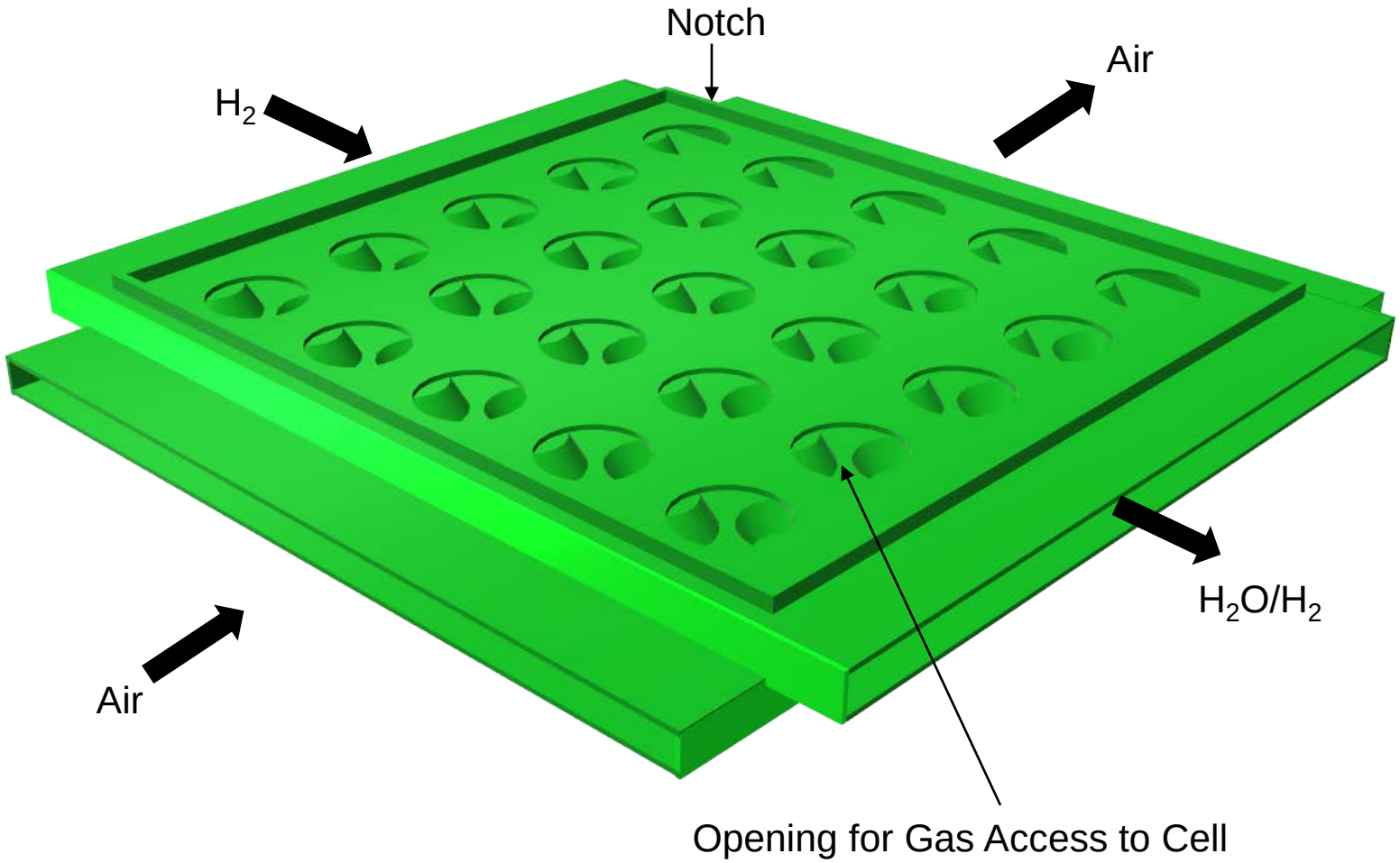




Not in Scale

Stack Design

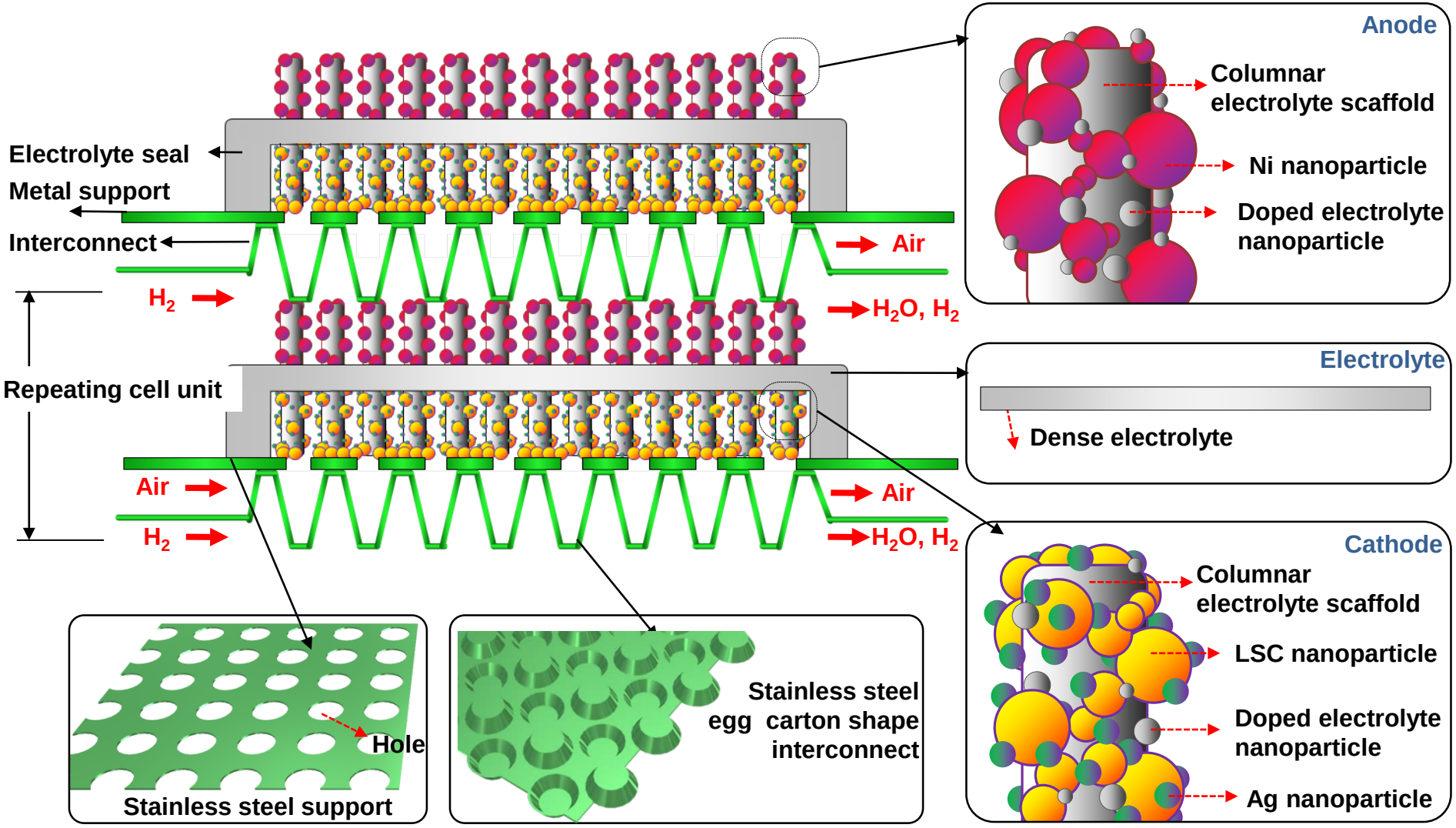
Cross Flow Gas Manifolding



Not in Scale

Stack Design

Incorporating Metal-Supported Cells



Project Technical Activities

- Prime surface interconnect design and fabrication development
- Metal-supported cell structure development
- Stack development
- Stack operation demonstration
- Stack cost assessment

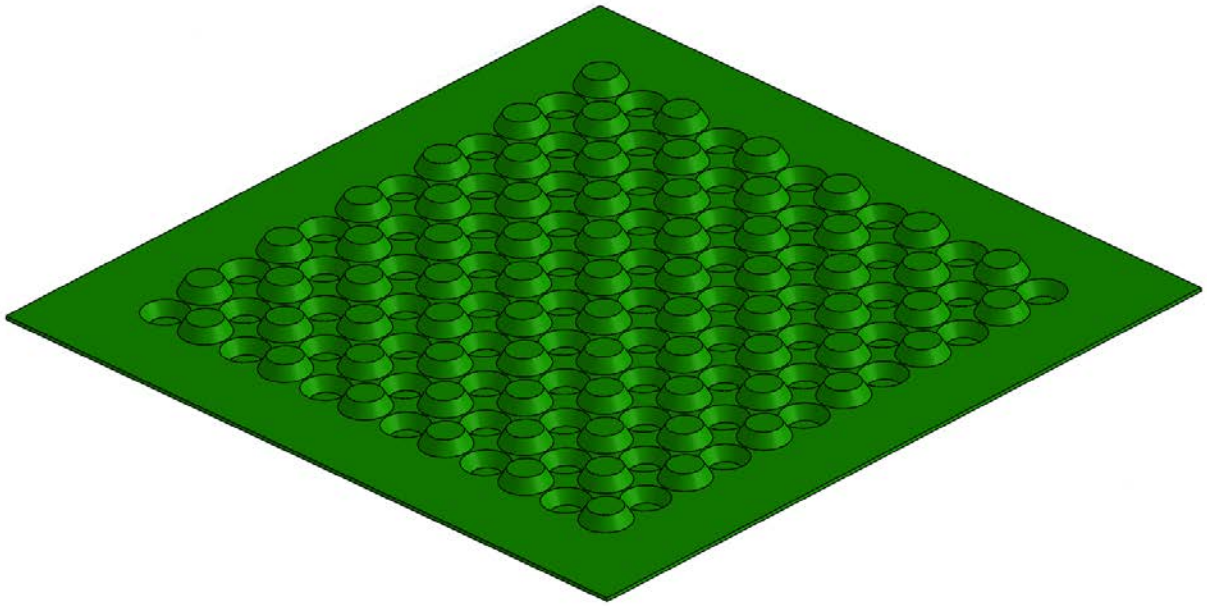
PRIME SURFACE INTERCONNECT DEVELOPMENT

Preliminary Interconnect Design Assessment

Preliminary design assessment in terms of

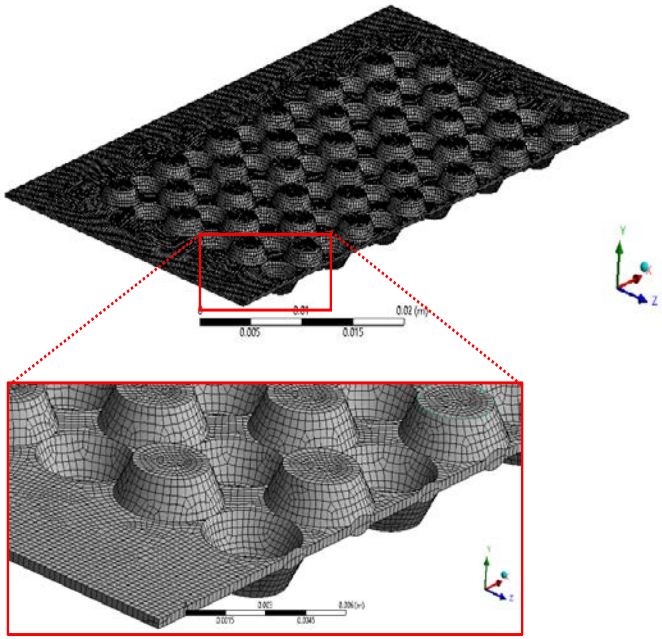
- Flow distribution
- Mechanical loading
- Current collection

Prime Surface Interconnect Design for Formability Evaluation

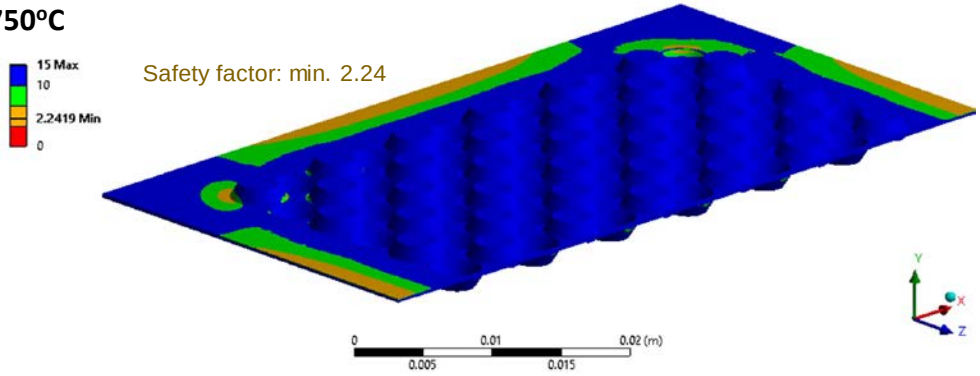


Dimension: Length x Width x Thickness	60mm x 60mm x 2.5mm
Thickness of the interconnect plate	0.3mm
Total height of the interconnect	2.5mm
Length of the interconnect	60mm
Width of the interconnect	60mm
Diameter of the cones at the base level	4mm
Cone angle	60 degrees
Mass of the interconnect	7.66 gram

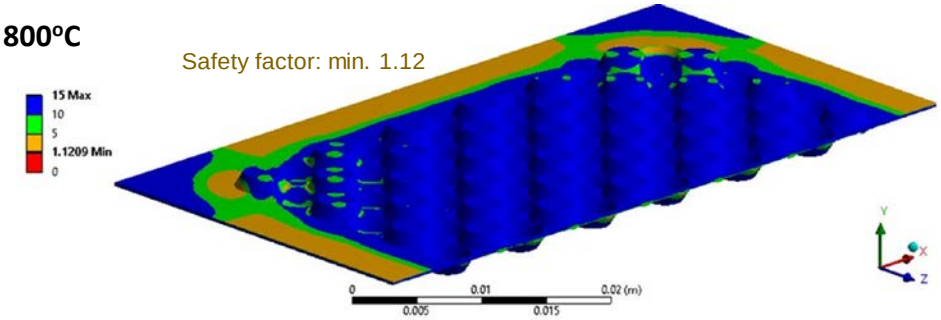
Mechanical Loading Investigation



(a) 750°C



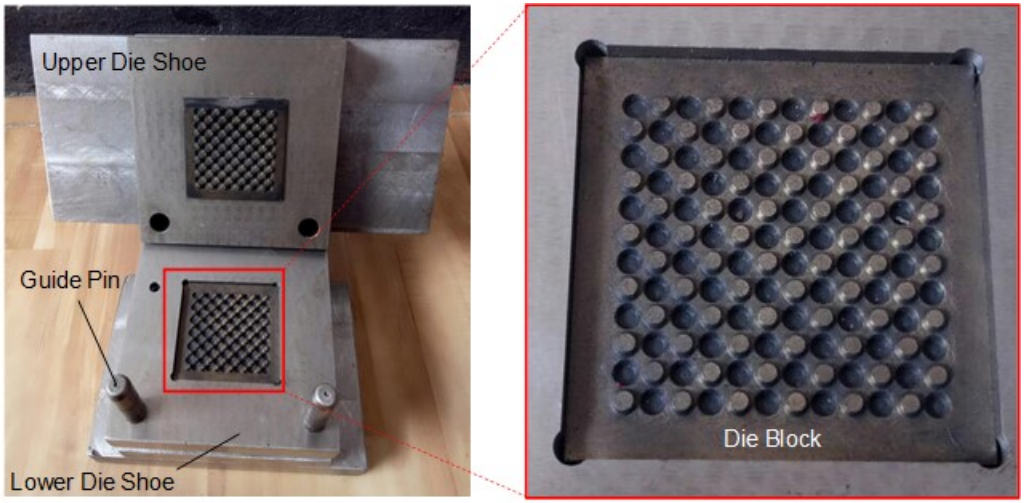
(b) 800°C



Interconnect Formability Investigation

- Hydroforming
- Stamping

Interconnect Stamping Investigation

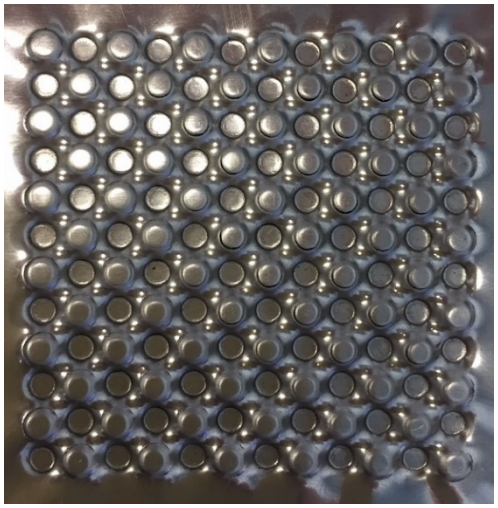


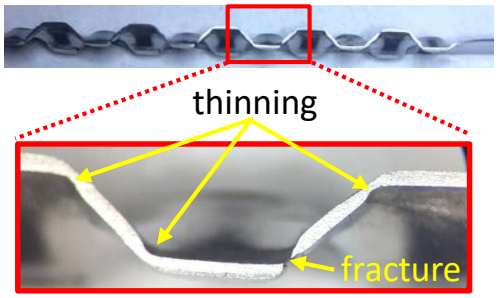
Key parameters investigated

- Height of interconnect,
- Thickness of interconnect,
- Distance between valley and hill,
- Cone angle.

Stamped Interconnect

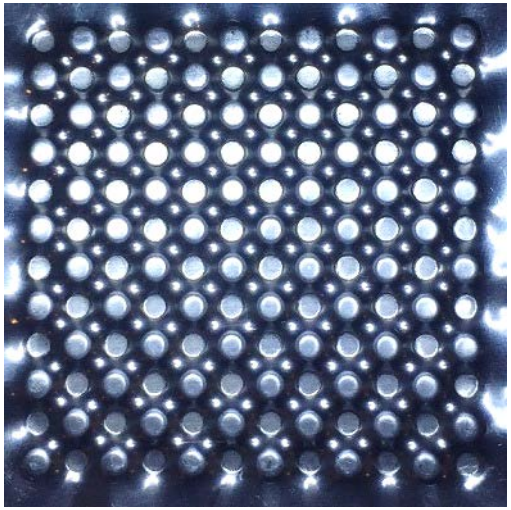
Interconnect with 2.5 mm in height

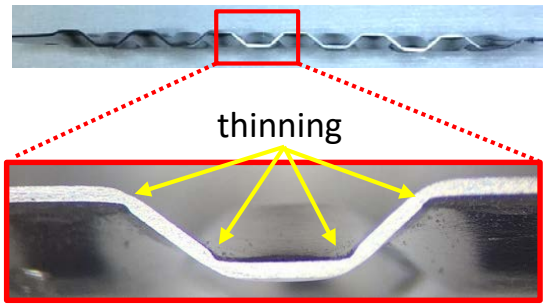




- Significant thinning
- Breakage at corners

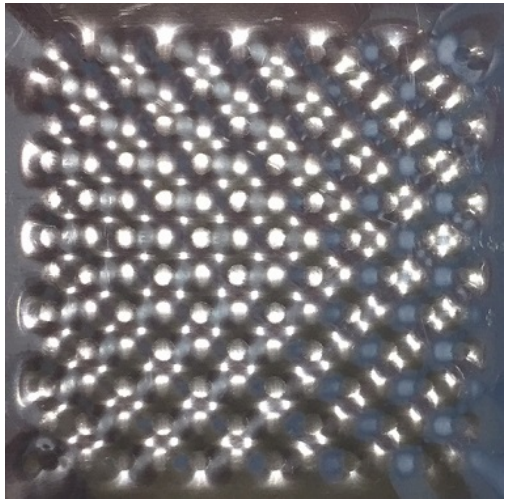
Interconnect with 2 mm in height

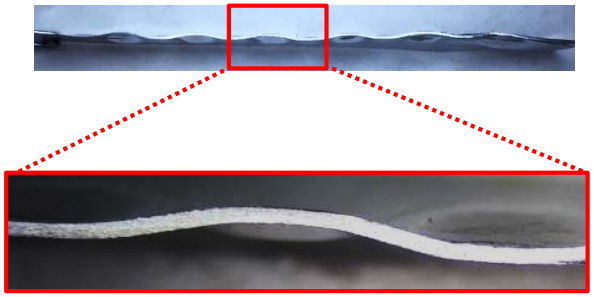




- Small thinning
- Well-formed egg-carton shape

Interconnect with 1 mm in height

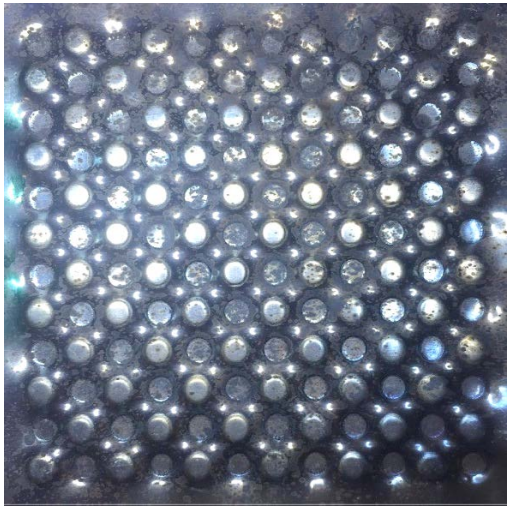


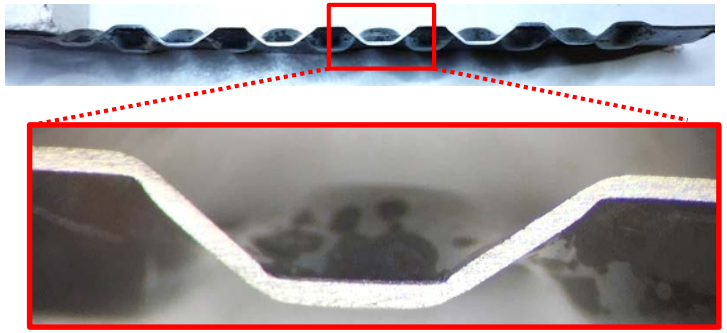


- No thinning
- Not well-formed egg-carton shape

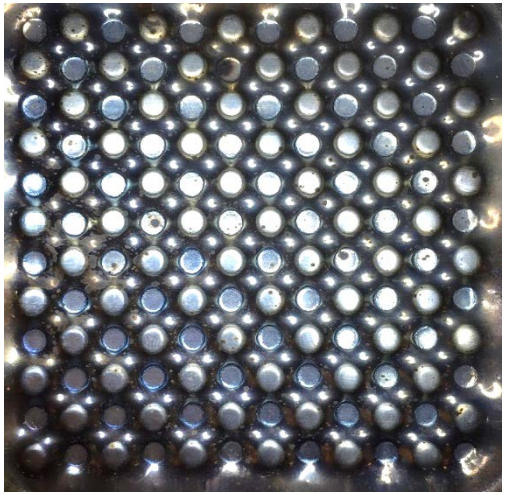
Preliminary Stamped Interconnect Characterization

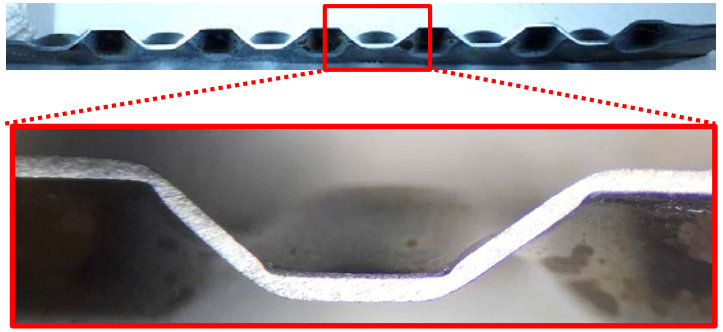
Interconnect with 2 mm in height after firing under load at 750 °C for 5 hours





Interconnect with 2 mm in height after firing under load at 800 °C for 5 hours



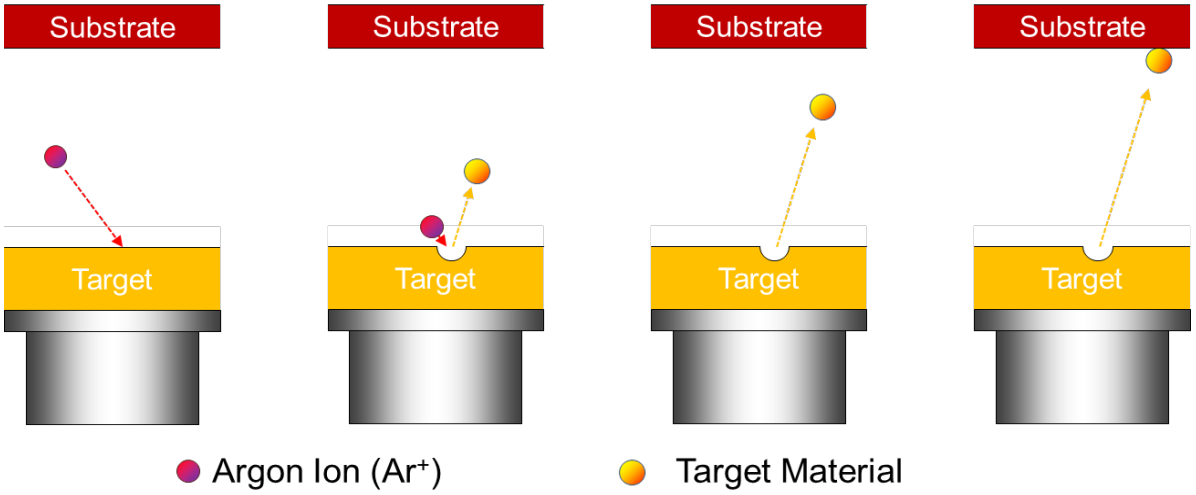


- no change on shape of egg-cartoon interconnects after sintering at 750 °C and 800 °C for 5 hours under load of 3 pounds (load of 100 cells and 100 interconnects)

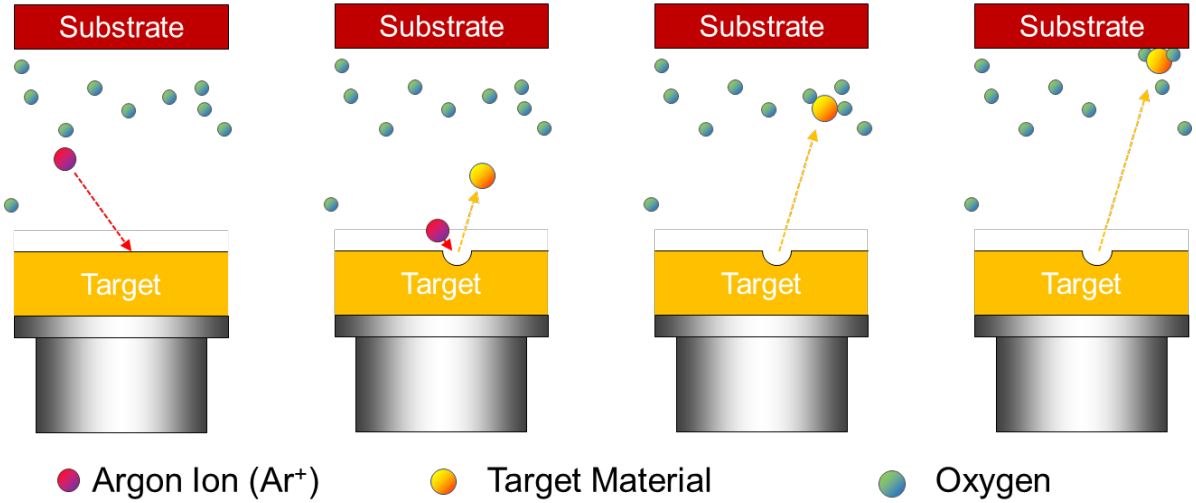
METAL-SUPPORTED CELL STRUCTURE FABRICATION

Sputtering Process

Conventional

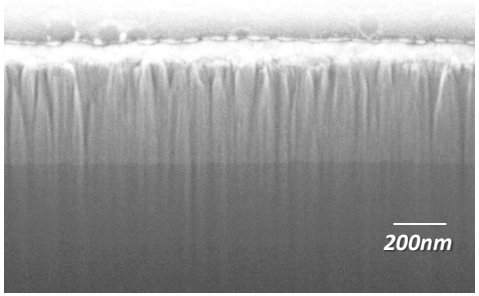


Reactive



Sputtering for SOFC Cell Fabrication

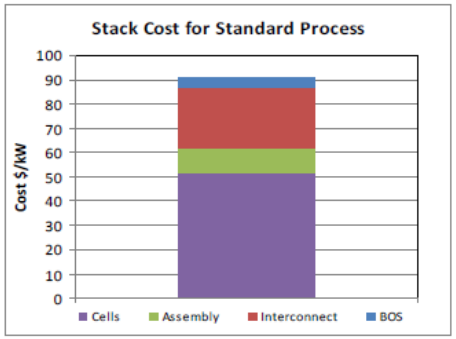
- Fabrication of dense and porous layers
- Scalability
- Potential cost effectiveness

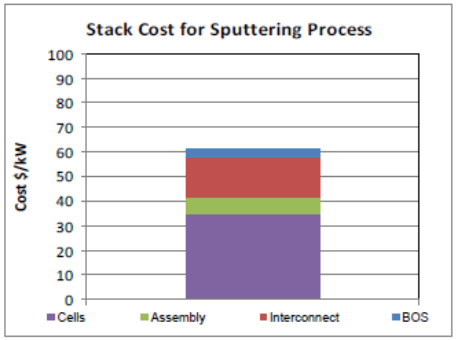


Nano-scale Dense YSZ layer

Goldstone Vacuum Sputter System
http://www.goldstone-group.com/

Sputtering Target by AZO Materials
http://www.azom.com/



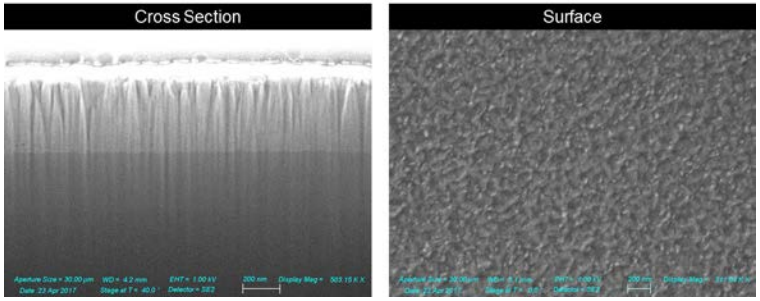


Weimar et al, PNNL Report PNNL-22732, 2013

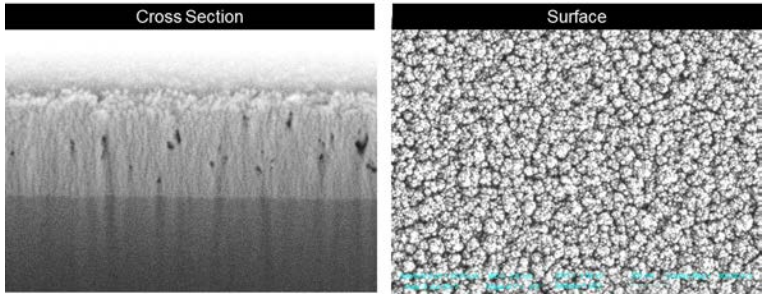
Cell Components and Single Cells Fabricated by Sputtering

(on Si wafers)

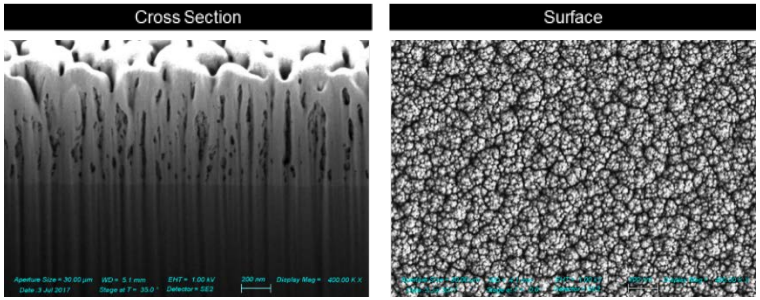
Dense YSZ Layer



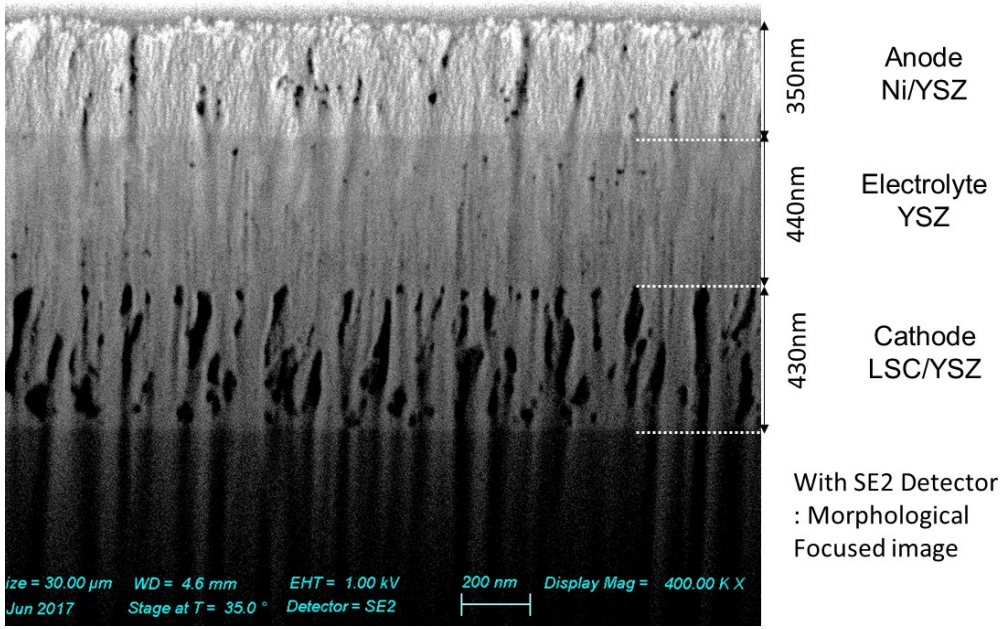
Porous Ni-YSZ Layer



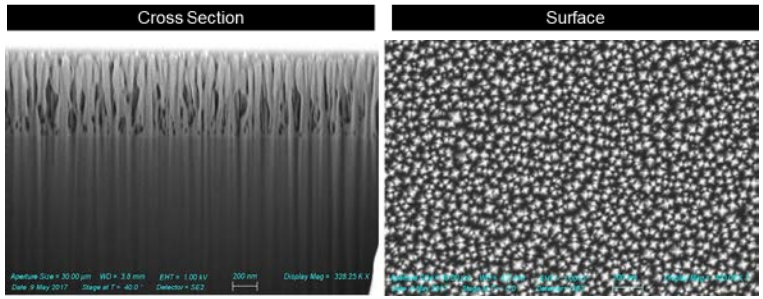
Porous LSCF-YSZ Layer



Single Cell

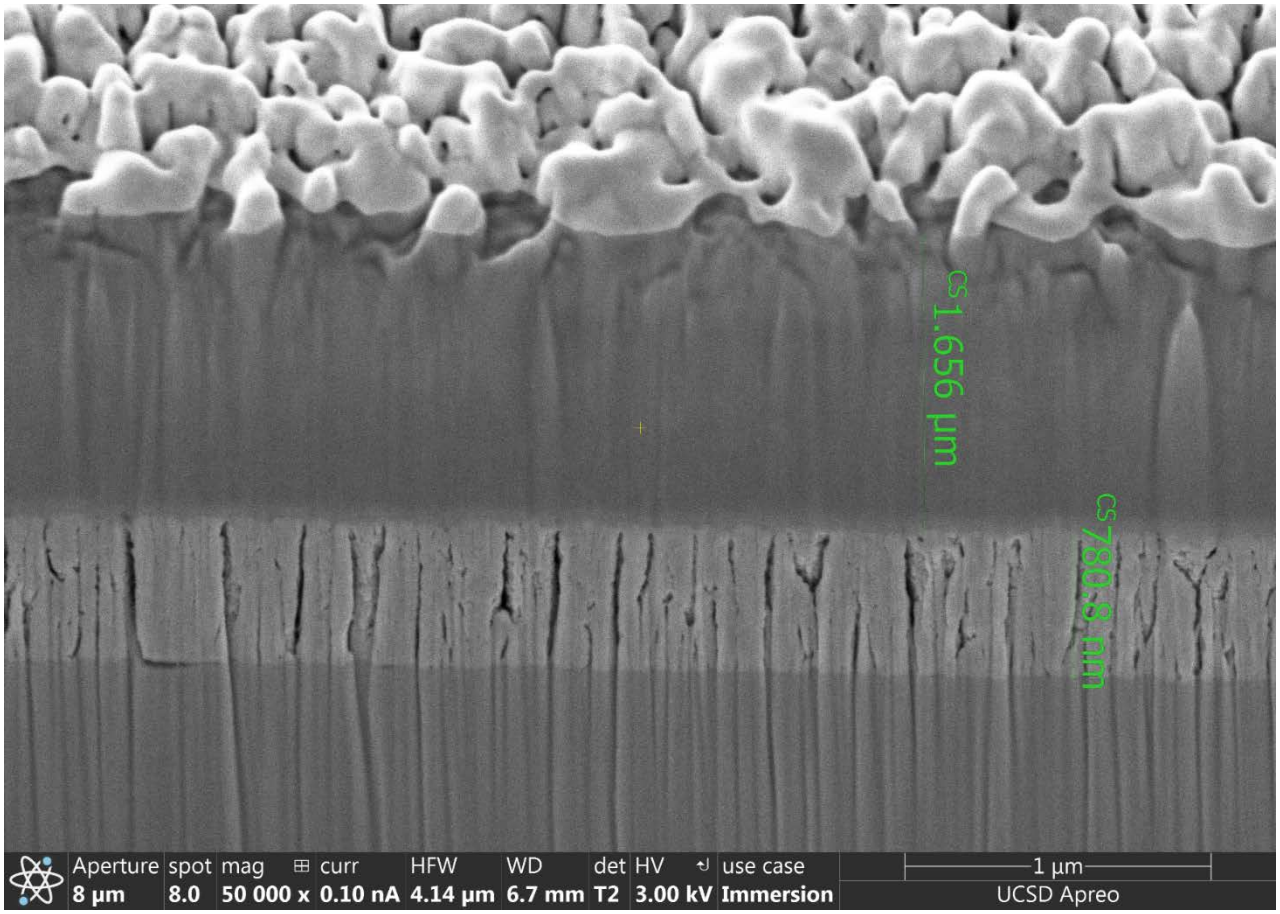


Porous LSC-YSZ Layer



Single Cell Fabrication

on Metal Substrate



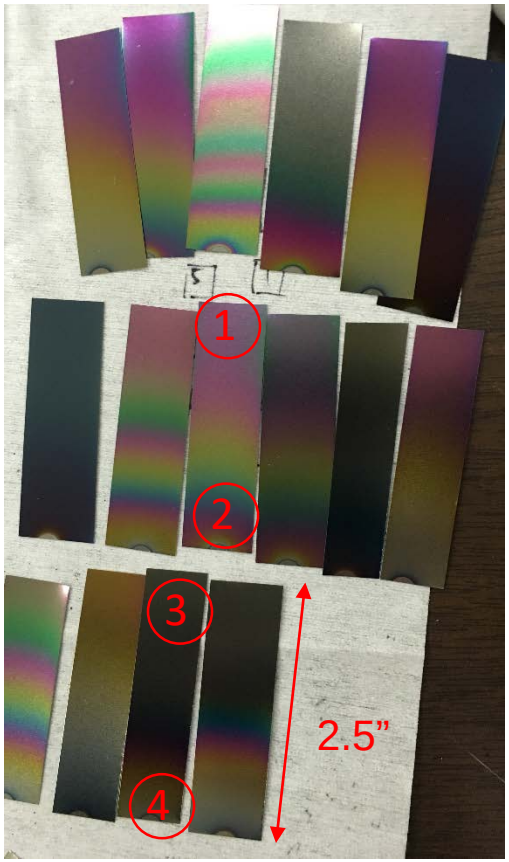
200nm — Cathode Pt

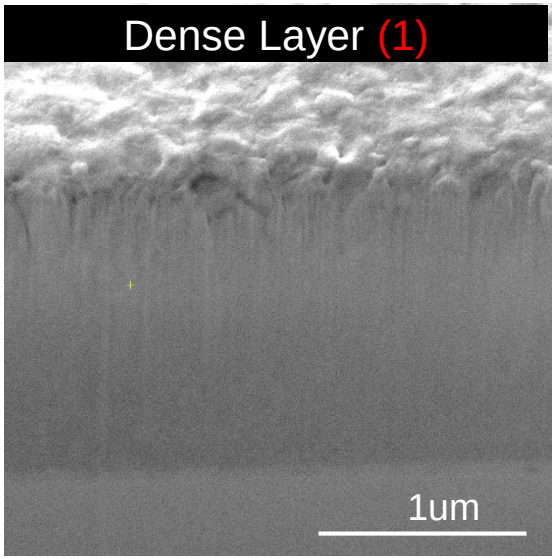
1.6um — Electrolyte YSZ

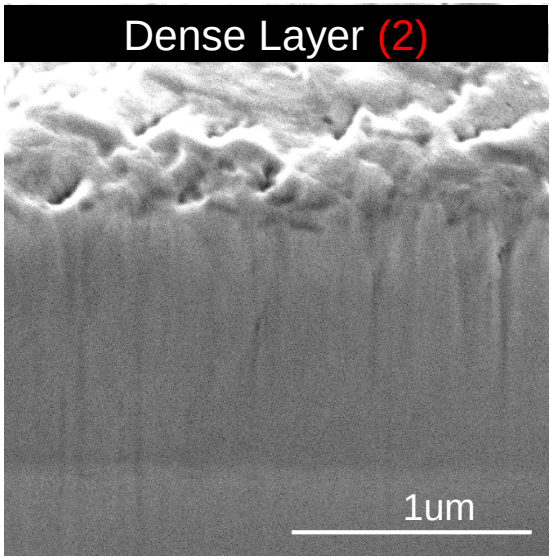
780nm — Anode Ni

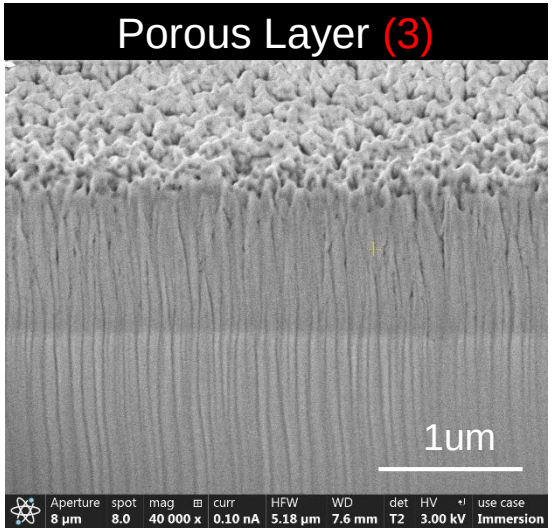
100um — Substrate Stainless Steel

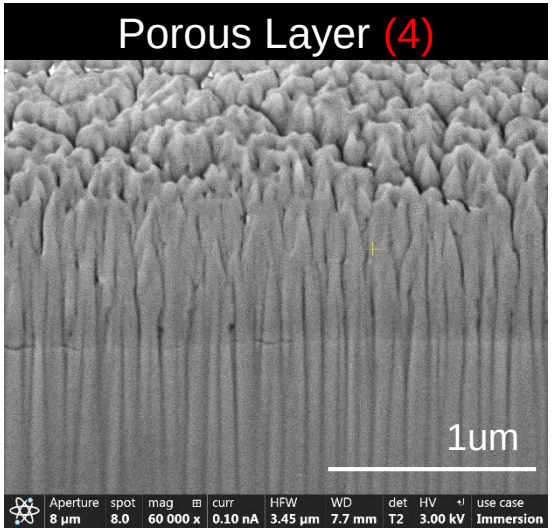
Single Cell Fabrication Scaleup



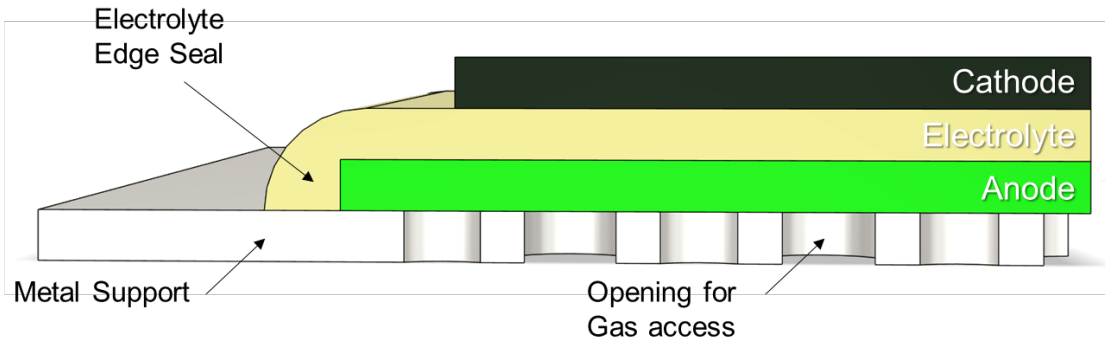


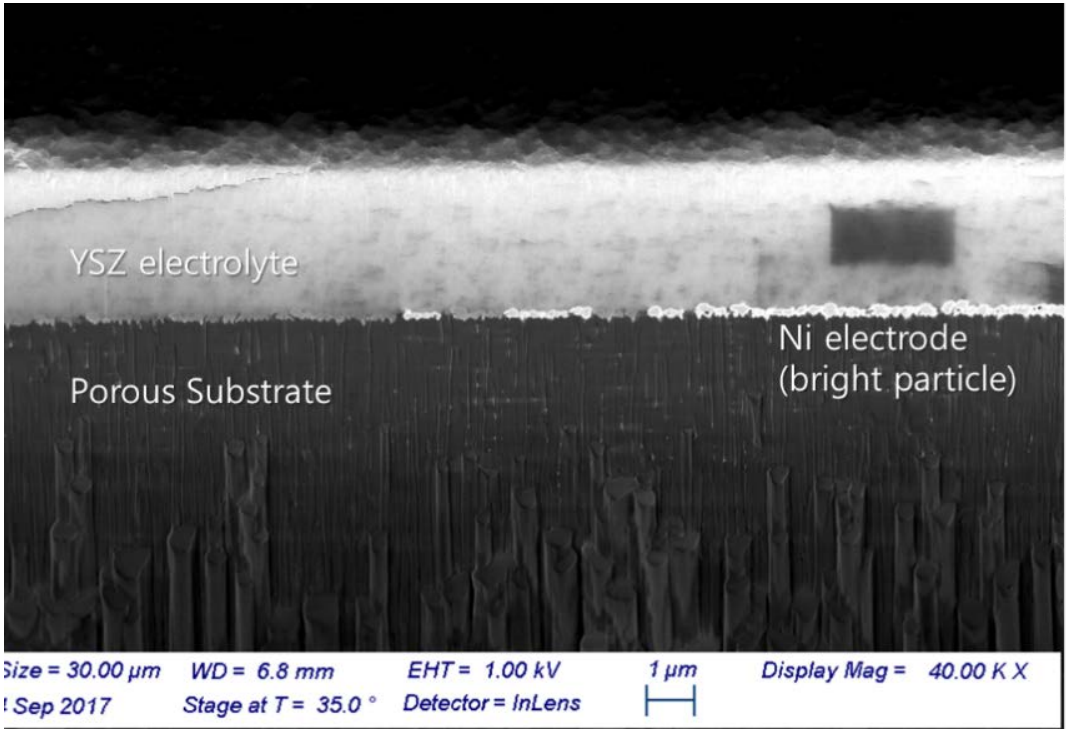






Cell Edge Seal

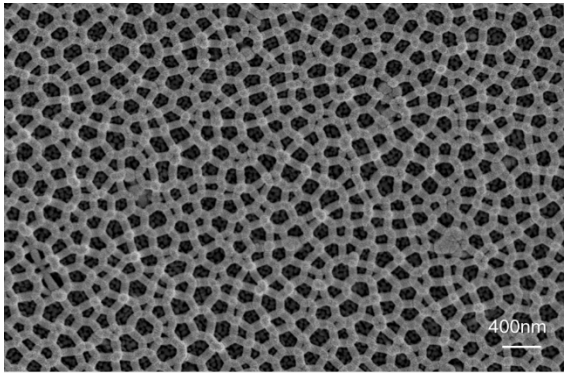




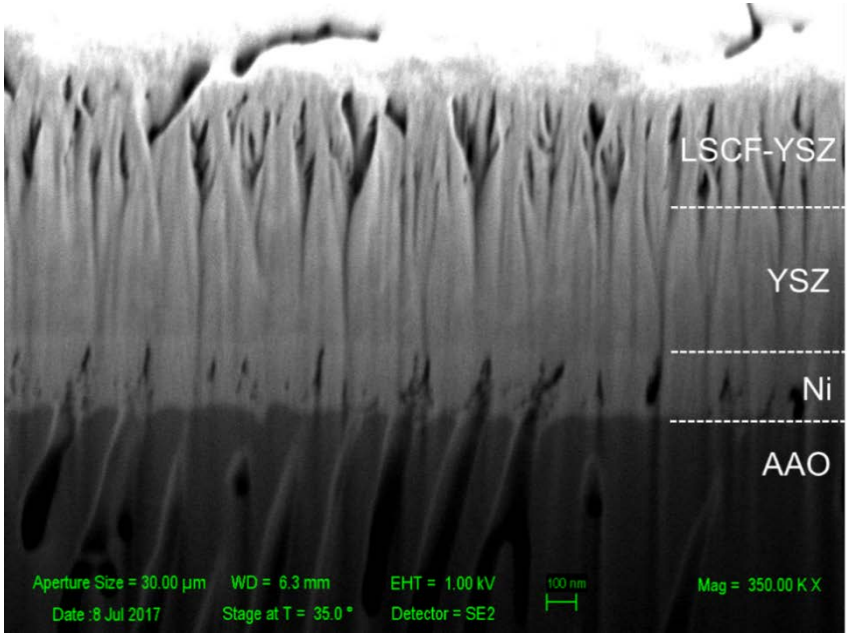
Single Cell Fabrication

on Anodizing Aluminum Oxide (AAO) Substrate

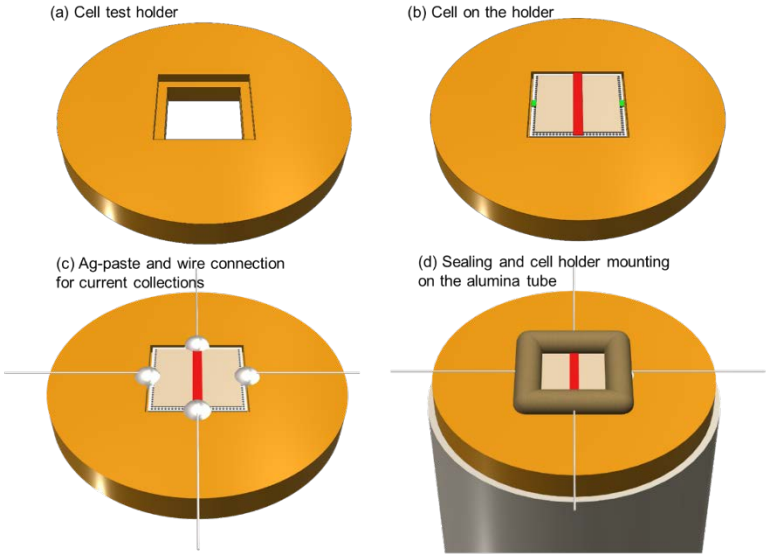
AAO Microstructure

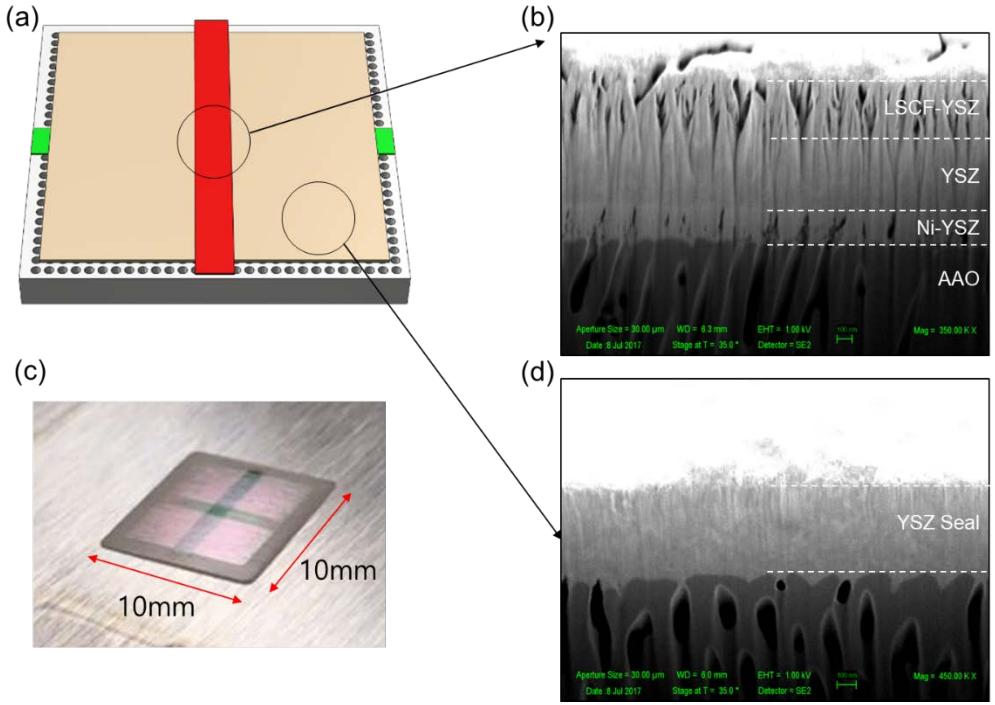


Single Cell

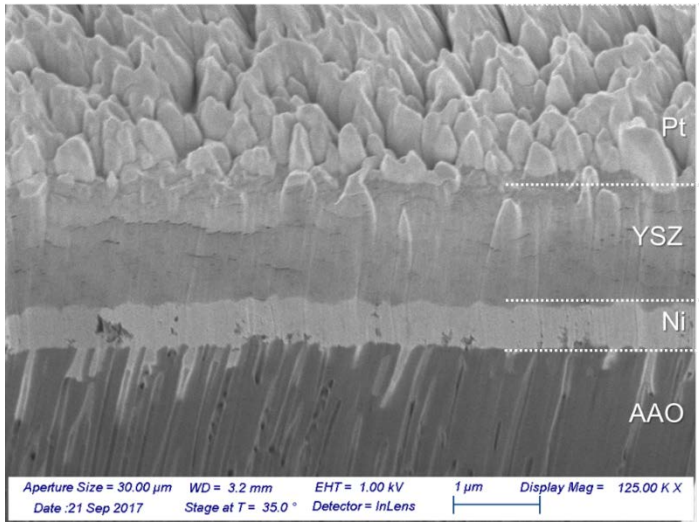


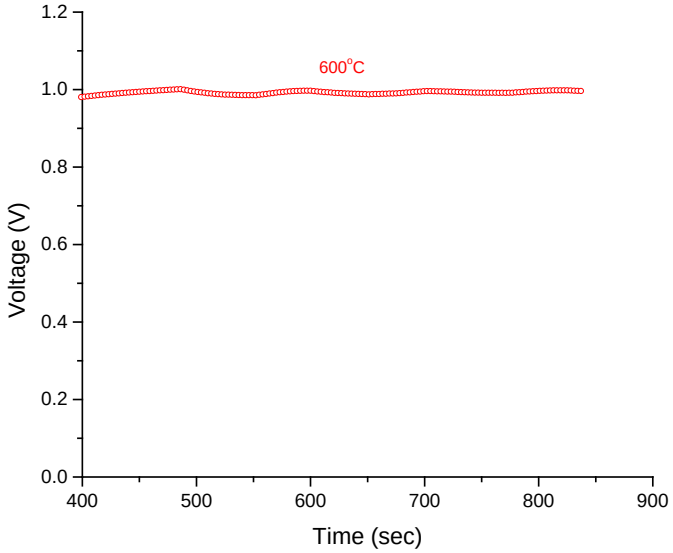
Cell Test Setup





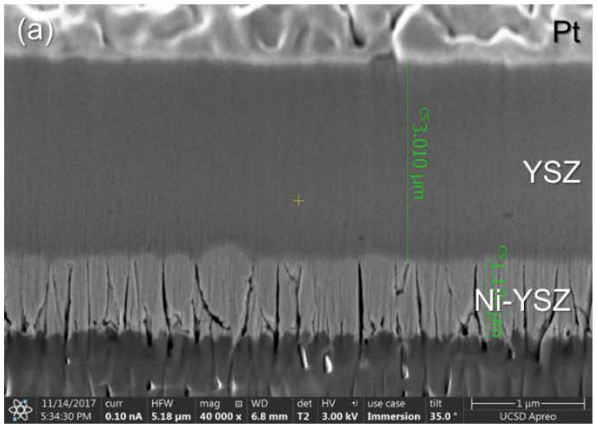
Cell Open Circuit Voltage

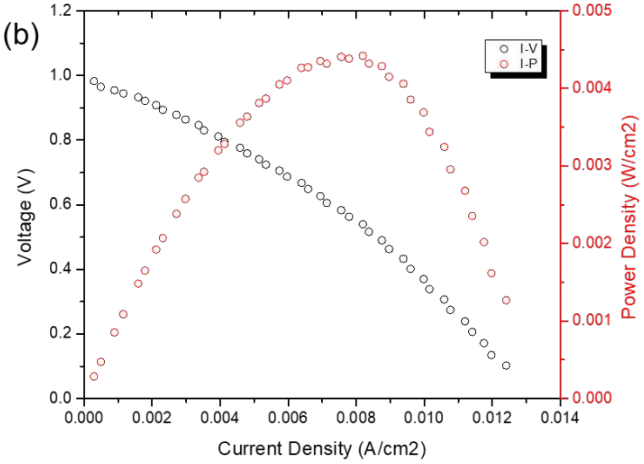




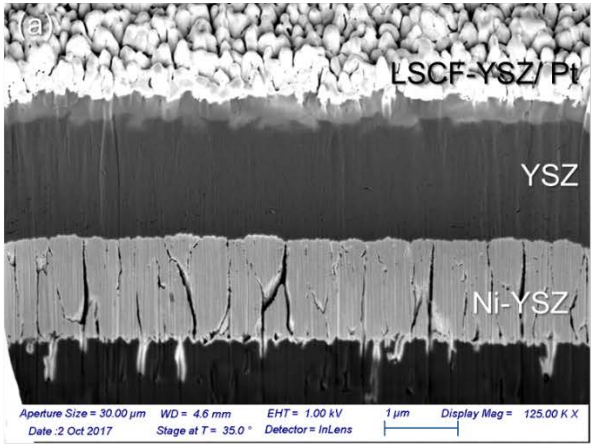
Initial Cell Performance

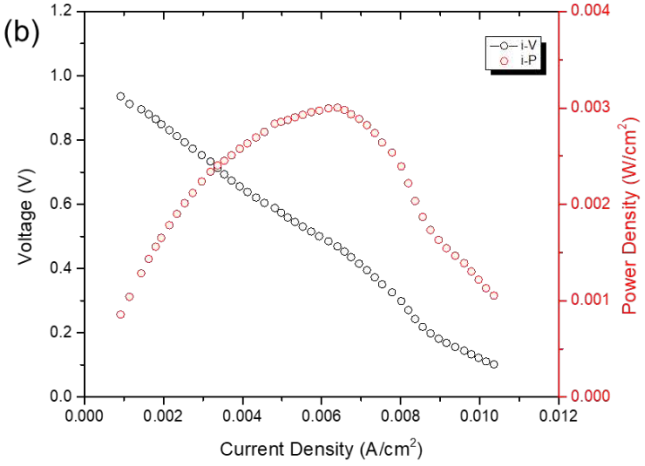
Pt/YSZ/Ni-YSZ





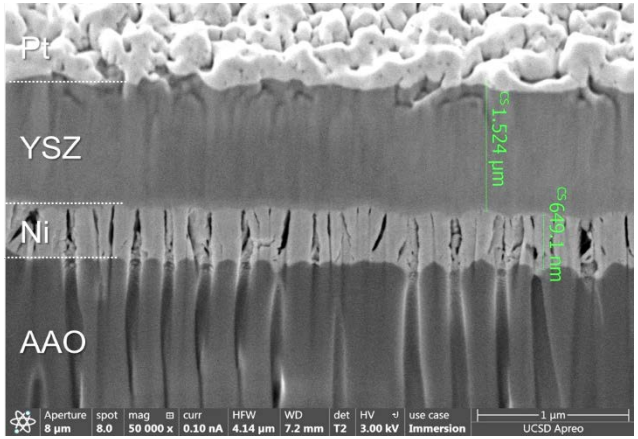
LSCF-YSZ/YSZ/Ni-YSZ

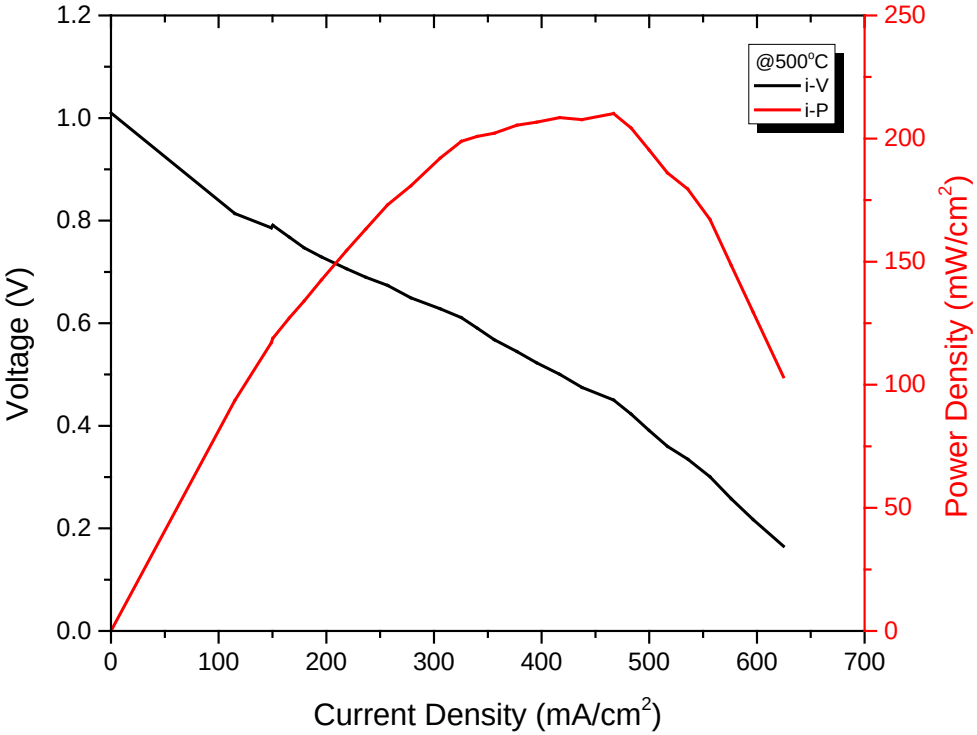


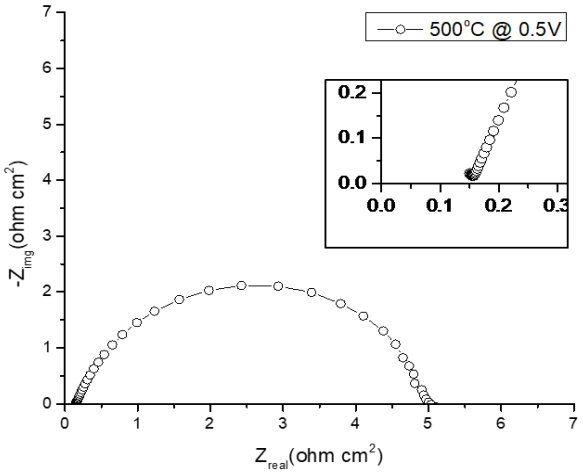


Single Cell Performance

on New AAO Substrate

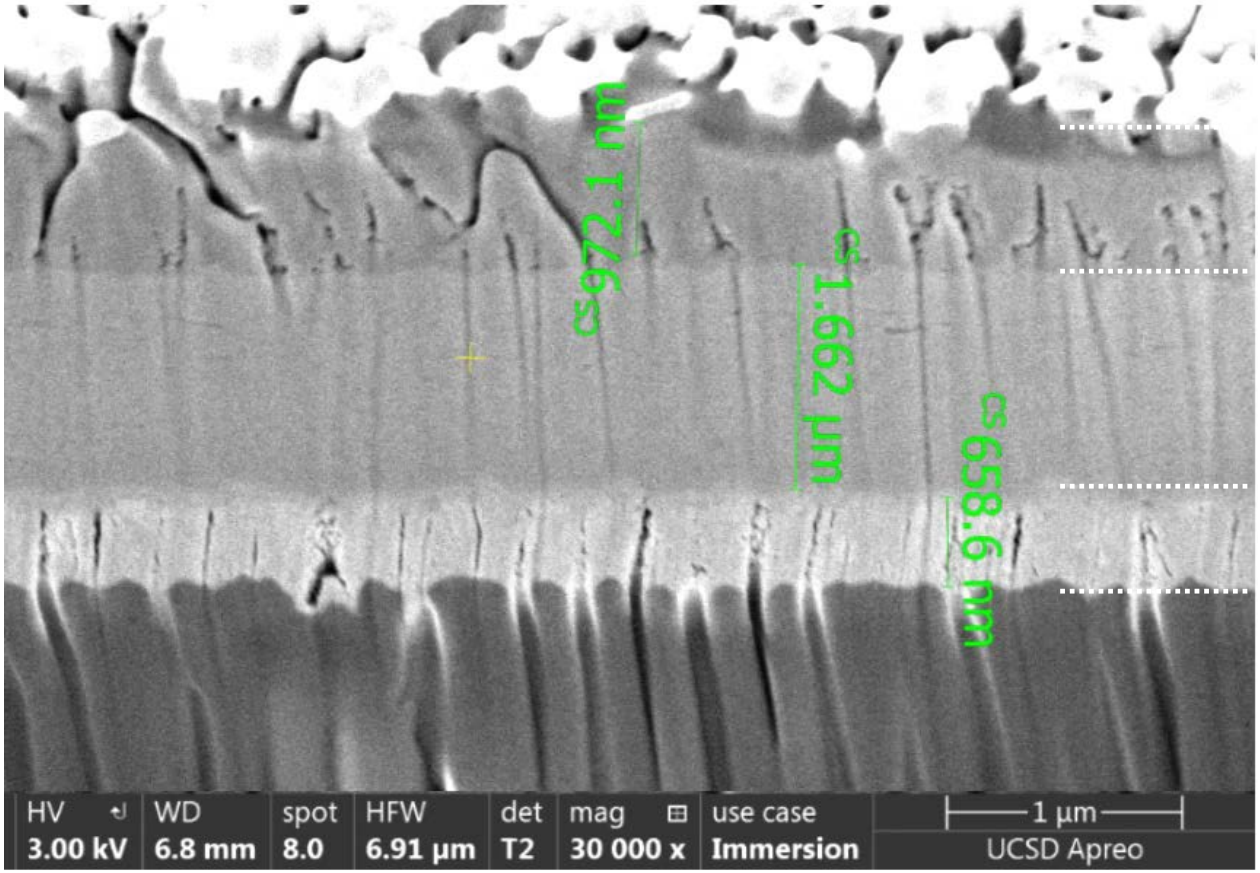






Single Cell Microstructure

(on new AAO Substrate)



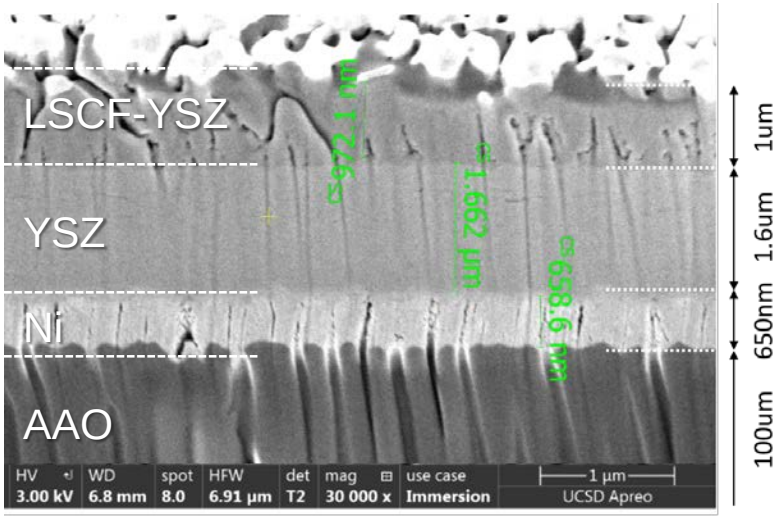
1um — Cathode LSCF-YSZ

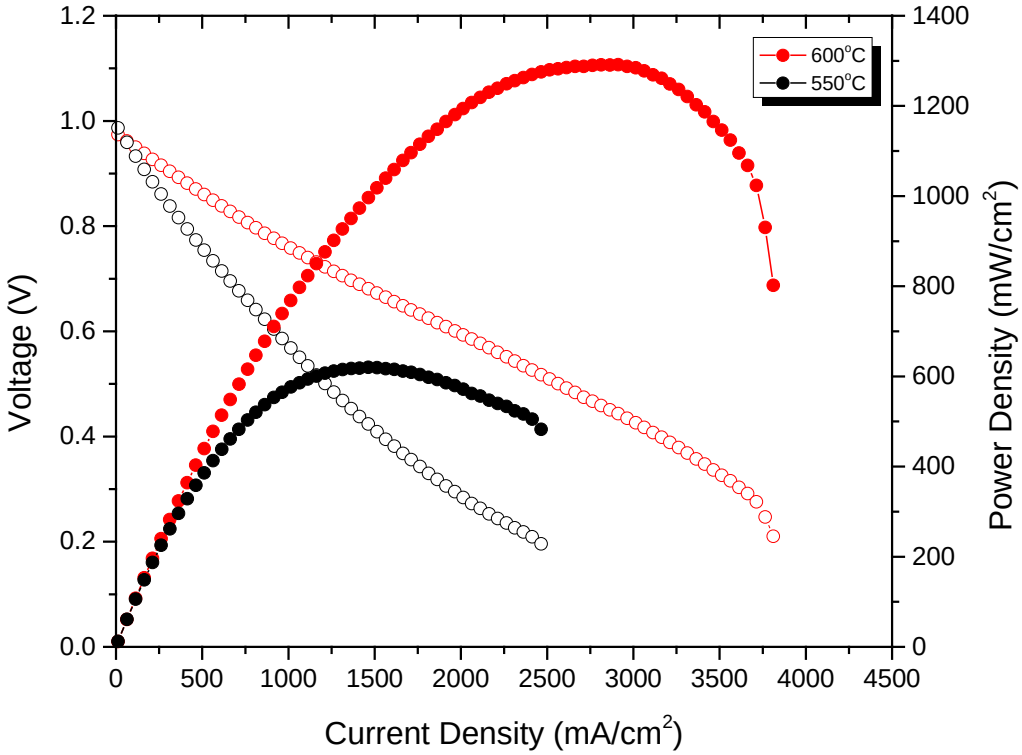
1.6um — Electrolyte YSZ

650nm — Anode Ni

100um — Substrate AAO

Cell Performance





Best performance reported on YSZ based cells at these temperatures

Summary of Key Results

- Preliminary interconnect design assessment and initial fabrication
- Demonstration of sputter processes for fabrication of cells with required microstructures and initial demonstration of process scaleup
- Demonstration of best performance to date for YSZ-based cells at reduced temperatures (1.3W/cm^2 at 600^{o}C)

Near-Term Future Work

- Prime surface interconnect development
  - Continue evaluation of stamping of egg carton shaped interconnect and characterize fabricated samples
  - Modify and optimize design and fabrication processes
- Metal-supported cell structure development
  - Optimize sputtering process and characterize fabricated cells
  - Demonstrate fabrication scale-up and performance of scale-uped single cells
  - Fabricate single cells on metal supports with openings
- Stack development
  - Initiate assembling of stacks incorporating prime surface interconnects

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