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Topical Report - Phase 1
(Final Report of Phase 1)

Deep Trek
Re-configurable Processor for Data Acquisition (RPDA)

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Abstract

This report summarizes technical progress achieved during Phase 1 (Feasibility Concept Definition and Proof of Concept) under the cooperative research agreement between Honeywell and U.S. Department of Energy to develop a high-temperature Re-configurable Processor for Data Acquisition (RPDA). The RPDA development will incorporate multiple high-temperature (225°C) electronic components within a compact co-fired ceramic Multi-Chip-Module (MCM) package. This assembly will be suitable for use in down-hole oil and gas applications. The RPDA module will be programmable to support a wide range of functionality. In particular this project will include demonstration of the RPDA configured to function as a Multi-Channel Data Acquisition Controller. This report addresses design requirements, electrical hardware design, MCM package design, and capability for manufacturing assembly, test and screening. Forward looking projection of cost/schedule performance and risk assessment lead to the conclusion that it is highly probable that Phase 2 objectives will be achieved.

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1.0 Glossary and Acronyms

AC Specifications	Refers to parameters that define periodic and/or transient performance characteristics (e.g., frequency, transition times, etc.).
A-to-D or ADC	Analog-to-Digital , or Analog to Digital Converter
Atmel	A commercial supplier of integrated circuits, including FPGA's. The High-temperature FPGA design that is used in this project is a fully-licensed high-temperature version of Atmel's AT6010 product.
Behavioral Model	Refers to a structured text-based representation of a design that defines circuit functional behavior using a "Hardware Description Language" (see HDL). A behavioral model may define a design or sub-block in terms of its inputs and outputs, functionality, and timing behavior. Behavioral models describe the design at a high level of abstraction and can be used to quickly capture and simulate operation of major system building blocks.
Configuration	In this context, refers to the process or data that defines the application-specific functionality of a Field-Programmable Gate Array (FPGA).
CCLK	Configuration CLocK: This is a signal generated within the HTFPGA that is used during the configuration of the device.
CMOS	Complementary Metal Oxide Semiconductor : A term generally applied to integrated circuit processes that use two types of field-effect transistors; employing n-channel (electron) and p-channel (hole) conduction. The n-channel transistors are turned on (conduct) by applying a positive gate voltage (relative to the source terminal), while p-channel transistors are turned on by applying a negative gate voltage.
DC Specifications	Refers to parameters that can be specified in terms of static conditions, without reference to any time dimension (e.g., standby current, static drive current, input/output voltage levels, etc).

1.0 Glossary and Acronyms (Continued)

Term	Definition
Die	An individual integrated circuit that has been cut from a silicon wafer (see “Wafers”).
DOE	Department Of Energy
DWD	Diagnostics-While-Drilling
EEPROM	Electrically Erasable Programmable Read-Only Memory: A memory device that can be used to store data by electrical means (programming), that retains such data even when power is interrupted, and that can also be erased (and subsequently re-written) by electrical means.
ESD	Electro-Static Discharge
FIFO	First-In, First-Out: Refers to a type of memory structure.
Foundry	A facility providing silicon wafer processing for 3rd party designs. As an adjective describes items that are used to support 3rd party designers (e.g., “foundry toolkit”).
FPGA	Field Programmable Gate Array: A digital device (Gate Array) where on-chip connections (and thereby functionality) can be defined and/or altered by the user in the field.
Gate Array	A component or design-style that makes use of predefined transistors and/or logic gate fabricated on silicon wafers where application-specific functionality is defined by the way in which the transistors or logic gates are interconnected.
Gate-level Model	Refers to a representation of a digital design that describes a circuit in terms of logic gates, flip-flops, or latches. Each of these circuit elements has a corresponding transistor-level design and physical layout that can be placed and routed within an integrated circuit.

1.0 Glossary and Acronyms (Continued)

GMS	General Manufacturing Standard: Nomenclature for Honeywell proprietary internal standards that specify recommended practices in various aspects of electronics development and manufacturing.
HDL	Hardware Description Language: Refers to one of several standard forms for describing integrated circuit behavior. Specific examples of HDL's are Verilog and VHDL.
HT2000 or HT2K	Refers to Honeywell's "High Temperature 2000" family of gate array products and/or design tools.
HTEEPROM	High Temperature EEPROM (see EEPROM)
HTFPGA	High Temperature FPGA (see FPGA)
HTSOI	High-Temperature Silicon-On-Insulator: An SOI integrated circuit manufacturing process that is optimized for extreme temperature applications (see SOI)
HTSRAM	High Temperature SRAM (see SRAM)
HW	Honeywell
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property: Frequently used to refer to designs and/or licenses that are procured for implementation.
Masks	See "Photo-masks"
Mentor	A software company that provides design automation software for the electronics industry

1.0 Glossary and Acronyms (Continued)

MCDAC	Multi-Channel Data Acquisition Controller: The name given to the RPDA after it has been programmed (i.e., configured) to implement the functionality defined within the appendix to this report. See “RPDA” and “configuration”
MCM	Multi-Chip-Module: An integrated circuit package that house multiple chips (or “die”).
MWD	Measurement-While-Drilling
NETL	National Energy Technology Laboratory – A division of the U.S. Department of Energy
Novacap	A commercial supplier of high-temperature ceramic chip capacitors
Non-volatile	In this context refers to a memory element or circuit that retains data content even if power is interrupted.
Objectives Specification	In this context refers to the document that was Phase 1 deliverable under the cooperative research agreement between Honeywell and DOE. This document defines the objectives of the hardware and hardware configurations for the RPDA to be accomplished in this project.
PGA	Pin-Grid Array: Refers to an integrated circuit package which is constructed such that signals are presented in a 2-dimensional array of pins that project from the package body. The pins can be inserted through holes on a board-level assembly.
Photo-masks	This is generally synonymous with “masks”(Sometimes also referred to as a “reticle”). A photo-mask is a glass plate with patterns that are transferred to silicon during wafer processing by shining ultra-violet light through the photo-mask onto a silicon wafer that has been pre-treated with light-sensitive coatings. Up to 27 different photo-masks may be involved in processing a single integrated circuit.

1.0 Glossary and Acronyms (Continued)

RMP	Research Management Plan: A report mandated by the cooperative research agreement between Honeywell and DOE.
RPDA	Re-configurable Processor for Data Acquisition: The generic name for the hardware module that is developed under this research agreement.
RTL	Register Transfer Level: Refers to a means of capturing the behavior of a digital integrated circuit in terms of the data that is stored in data registers. Such a description is like a state-machine where the state changes with each clock cycle. Data is transferred between on-chip registers synchronously using one or more system clocks. An RTL description defines the registers, and how their contents are determined from one clock cycle to the next.
SRAM	Static Random Access Memory: A memory device in which data is stored at specific addresses where these addresses can be accesses in any sequence (i.e., randomly) by forcing address input bits to the desired state. A "static" memory means that a clock does not have to be running in order for the device to retain data (as opposed to a Dynamic Random Access Memory, or DRAM, which requires a clock or a minimum operating speed to function properly).
SOI	Silicon On Insulator: An integrated circuit device structure where all the transistors/devices are individually isolated by a silicon dioxide insulating layer as opposed to silicon p-n junction isolation.
SOPO	Statement Of Project Objectives: The section in DOE's agreement with Honeywell that defines the tasks to be completed on the program.
SPI	Serial Peripheral Interface: Refers to a commonly used protocol that establishes means for serial data communication between a master and multiple slave devices.

1.0 Glossary and Acronyms (Continued)

SPICE	A generic name for a variety of commercially available circuit simulation programs. Electrical behavior is modeled at the device level (i.e., circuit elements are transistors, resistors, capacitors, etc.)
SRAM	Static Random Access Memory. Refers to a data memory circuit where the data can be randomly accessed by means of the data "address" inputs. "Static" refers to the fact that the memory retains data as long as power is applied without any requirement for periodic "refreshing" (i.e., re-writing) the data.
Synthesis	In this context, synthesis refers to the process of creating a Gate-level Model of a design that is functionally equivalent to a Behavioral or Register-Transfer-Level (RTL) representation of that design.
TBD	To Be Determined
TSA	Technology Status Assessment: A report mandated by the cooperative research agreement between Honeywell and DOE.
Volatile	In this context, refers to memory or a circuit that can store data as long as power is applied, but where that data is lost if power is interrupted.
Wafers	Specially prepared sections of single-crystal silicon that are processed to produce integrated circuits. Wafers on this program have a 6-inch diameter and are approximately 675 microns thick. Many individual integrated circuits are produced on a wafer and these are cut apart at the completion of wafer processing.
WBS	Work Breakdown Structure

2.0 Executive Summary

High-reliability, high-temperature packaging is an essential element of down-hole electronic systems. Co-fired ceramic Multi-Chip Modules (MCM's) can meet this need with stable performance at temperatures greater than 225°C.

Under this project, Honeywell is developing an MCM to house several High-Temperature Silicon-on-Insulator (HTSOI) integrated circuits and nine ceramic chip capacitors in a package with 147 pins. The physical design of the package is tailored to down-hole applications in terms of physical dimensions, wide operating temperature range, and ability to withstand high shock and vibration environments. The integrated circuits included in the package are chosen to provide capability equivalent to a simple, flexible micro-controller with built-in non-volatile instruction memory and data memory in a single package. The first usage of this module will be achieved by configuring it as a Multi-Channel Data Acquisition Controller (MCDAC) that can be used with other HTSOI components developed for down-hole data acquisition applications. This intended application leads to the title of this project, *Reconfigurable Processor for Data Acquisition,* or RPDA.

The integrated circuits have been previously developed and are fabricated using silicon on insulator process technology specifically developed for extreme temperature applications. The high-temperature wafer process and two of the HTSOI integrated circuits were developed under a recently completed DeepTrek cooperative research agreement (DE-FC26-03NT41834). The three integrated circuits are a 32K word by 8-bit non-volatile memory (HTEEPROM), a 32K word by 8-bit static RAM (HT6256 SRAM), and a 30,000 gate high-temperature field-programmable gate array (HTFPGA). This last component (HTFPGA) is the key programmable element within the RPDA. It has been developed as a high-temperature functional equivalent to a conventional temperature range commercial field-programmable gate array (FPGA), the Atmel AT6010.

An MCM can be likened to an electronics board implemented in a single solid piece of ceramic material. Layers of ceramic material (Alumina, Al_2O_3) are alternated with patterned layers of interconnect metallization (such as Tungsten) that are built into a multi-layered structure and then fired to result in a single, hermetic ceramic package. Multiple die can be housed in such a package using high-temperature adhesives and wire-bonded to internal package interconnect traces. External pins will be brazed onto the ceramic body where external metallization is plated with gold for long-term high-temperature applications. Lids made of Kovar (Ni-Fe-Co) that are well matched to the thermal expansion properties of the ceramic can be welded to Kovar seal rings built into the ceramic. This technology results in high density, hermetically sealed packaging with short internal wire lengths that is extremely tolerant of shock and vibration and capable of withstanding extreme temperature cycles.

This report summarizes Phase 1 development (Feasibility Concept Definition and Proof of Concept) of the RPDA. The aim of this Phase 1 activity is to define at a high level of detail the objectives and the technical approach to implementation, and then to follow up with design and analysis to show that the concept is valid and that the implementation plan can be successfully carried out. This report is intended to show that this is true in the case of the RPDA.

This program was initiated on Oct 1, 2006. During Phase 1 a Technology Status Assessment (TSA) was delivered to address the need for this project and describe the current status of technology available to serve the need. An Objectives Specification has been delivered defining in detail the intended development outcome. A Research Management Plan (RMP) has also been delivered that addresses the project tasks, resources, timeline, and funding requirements.

The Research Management Plan divided Phase 1 activity into several tasks. These include:

(1) Generation of the Objectives Specification;

(2) Digital Sub-system Specification and Design, which incorporates all of the activity associated with defining the electrical connectivity of the hardware, analyzing performance and developing target electrical performance specifications, and definition of targeted Multi-channel Data Acquisition Controller (MCDAC) function; demonstration by simulation and analysis of means for programming the RPDA (i.e., configuring the embedded HTFPGA), and demonstration by simulation and analysis the means for configuring the RPDA to implement the targeted MCDAC functionality

(3) MCM package Design and layout; including specification of materials, construction, components, physical dimensions, component placement, electrical connectivity, and means for signal and power routing. This task also addresses assembly and screening process requirements to ensure the manufacturability of the RPDA as commercial product.

(4) Test Specification; including development of test strategies to ensure comprehensive test capability for demonstration, qualification, and manufacturing test.

Phase 1 technical tasks are substantially complete and project objectives are being met. Administrative tasks and report have been completed per the schedule of deliverables. Phase 1 technical accomplishments include:

- MCM package design is complete
- Preliminary bills or material and assembly process flows have been completed
- RPDA hardware electrical design and analysis has been completed
- HTFPGA simulation databases have been developed and verified
- HTFPGA configuration tools and procedures have been installed and verified
- HTEEPROM / HTFPGA configuration issues have been detected (via simulation) and corrective action identified and implemented
- Top-level simulation of the RPDA has been completed including verification of configuration and post-configuration behavior
- Specification and synthesis of Multi-channel Data Acquisition Controller (MCDAC) functionality has been achieved and configuration tools successfully run to configure the RPDA for MCDAC functionality
- Test flows have been defined and test capability assessed with positive results
- Preliminary test plans and procedures have been documented.

With this level of development successfully completed it is reasonable to proceed with prototype fabrication and hardware demonstration as proposed for program Phase 2.

3.0 References

1. RMP-NT42947: Research Management Plan for Deep Trek Re-configurable Processor for Data Acquisition, December 4, 2006.
2. TSA-NT42947: Technology Status Assessment for Deep Trek Re-configurable Processor for Data Acquisition, February 26, 2007
3. Data Acquisition System Objectives Specification: for Deep Trek Re-configurable Processor for Data Acquisition, January 31, 2007.
4. GMS-10030/A, General Manufacturing Standard for Multi-Chip Module Package Design, Honeywell Proprietary internal documentation, 8-5-1996.
5. GMS-10022/H, General Manufacturing Standard for Integrated Circuit Design, Honeywell Proprietary internal documentation, 9-28-2006.
6. Atmel *“Field Programmable Gate Array Configuration Guide”* for AT6000 Series Devices, dated 9/99
7. Honeywell *“HT2000 Data Book”* revision 11-11-2005.

4.0 Results and Discussion

The overall technical approach for this project is described within the Research Management Plan (reference 1). To briefly re-state, that approach involves developing an RPDA hardware module based on previously developed High-temperature integrated-circuit components consisting of: an SRAM (static random-access memory); an EEPROM (electrically-erasable programmable read-only memory); and an FPGA (field-programmable gate array). This involves specification and development of a ceramic multi-chip module (MCM) package to house these components. The project further embodies developing a configuration file for the FPGA, and demonstrating the ability to embed the configuration file within the EEPROM in such a way that the RPDA module autonomously configures itself on power up. The project further involves developing test hardware and software for the RPDA. Additional detail regarding the technical approach is contained within the Objectives Specification (reference 3).

The remainder of this Results section is in an outline format that may be considered as a check-list roughly organized to ensure that:

(1) Requirements have been adequately defined and documented;
(2) Electrical design and analysis has been completed to address the requirements, including capability for application of tools and procedures to configure the hardware;
(3) The electrical design architecture lends itself to comprehensive testing;
(4) The MCM package has been specified and designed to meet the objectives;
(5) The MCM design has been analyzed relative to thermal, mechanical, and electrical performance considerations;
(6) Viable processes exist to assemble the MCM sub-components into a completed configuration in a manufacturing environment;
(7) The assembled module is compatible with high-temperature test, qualification and screening in a manufacturing environment;
(8) The completed assembly can be expected to meet perform reliably for the intended end use;
(9) Multi-Channel Data Acquisition Controller functionality is defined for prototype demonstration and can be implemented using available configuration tools and procedures.

4.1 Design Requirements

Overall design objectives were defined in the Objectives Specification (reference 3). This includes physical dimensions, hardware design architecture, input/output configuration, environmental operating requirements, and target functionality for demonstrating configuration (i.e., programming) of the RPDA. No changes have been made to these general requirements. In other words, the design progress to date is fully compliant to the Objectives Specification.

4.1.1 Operating Conditions

Operating conditions are defined per the Objectives Specification and are shown in Table 1.

Table 1: RPDA Recommended Operating Conditions

Parameter	Limits			Units
	Min	Typical	Max	
Positive Supply Voltage	4.75	5.0	5.25	Volts
Voltage On Any Pin (1)	-0.3		V_{DD}+0.3	Volts
Capacitive Output Load			TBD	pF
Case Operating Temperature	-55		225	°C

(1) TM_VP and TM_VM pins are exceptions when data is being written to the HTEEPROM (these pins are listed in Table 3 as package pins c21 and e21 respectively) . These pins are connected to the HTEEPROM internal charge-pumps and will typically be at +8.5V (VP) and -8.5V (VSS) during HTEEPROM write operations. Otherwise, during normal operation they are constrained to the voltages in the above table.

4.1.2 Absolute Maximum Ratings

Absolute Maximum Ratings are defined per the Objectives Specification and are shown in Table 2. **Note:** Due to HTEEPROM data-retention considerations, storage temperature has been reduced to 250°C (from 325°C in the Objectives Specification).

Table 2 - Absolute Maximum Specifications

Symbol	Parameter	Ratings[1]		Units
		Min	**Max**	
V_{DD}	Positive Supply Voltage (2)	-0.5	6.5	Volts
V_{PIN}	Voltage on Any Pin (2, 5)	-0.5	V_{DD} + 0.5	Volts
I_{OUT}	Average Output Current	-20	20	mA
T_{STORE}	Storage Temperature	-65	**250**	°C
T_{SOLDER}	Soldering Temperature (5 seconds)		355	°C
P_D	Package Power Dissipation (3)		3	W
$Ø_{JC}$	Package Thermal Resistance 147 PGA MCM (Junction to Case)		7.0	°C/W
V_{PROT}	Electrostatic Discharge Protection Voltage (4)	2000		V
T_J	Junction Temperature		300	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to V_{SS}
(3) RPDA power dissipation due to I_{DDS}, I_{DDOP}, and I_{DDSEI}, plus RPDA output driver power dissipation due to external loading must not exceed this specification
(4) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015. This is goal. ESD withstand capability has not been established for all of the components (as of Jan. 31, 2007).
(5) VP and VM test pins are exceptions when data is being written to the HTEEPROM. These pins are connected to the HTEEPROM internal charge-pumps and will typically be at +8.5V (VP) and -8.5V (VSS) during HTEEPROM write operations. Otherwise, during normal operation they are constrained to the voltages in the above table.

4.1.3 Design Process

The Multi-Chip Module (MCM) package design has been completed in conformance with Honeywell's internal MCM design process requirements (Reference 5). In addition the MCM physical construction is designed for compliance to the current revision of layout rules in place with Honeywell's chosen MCM package vendor. The electrical

design has been assessed according to applicable criteria extracted from Honeywell's internal integrated circuit design process (Reference 6).

4.2 Hardware Electrical Design

4.2.1 Circuit Overview

The electrical design incorporates three High Temperature Silicon-on-Insulator (HTSOI) integrated circuits and nine ceramic chip capacitors in a ceramic package with 147 pins. MCM dimensions are 2.2" x 0.75". There are up 112 programmable I/O. This includes up to 55 fully configurable I/O plus 57 I/O with direct access to SRAM/EEPROM bus that can also be configured by the user. The design, materials and construction support operation at 225°C, and storage at 250°C. The module operates at system clock rates upt to 10MHz from a single 5V supply and utilizes CMOS I/O levels. Multiple mode programming can be performed (using configuration modes 1, 2, and 5 as defined within Reference 7)

The internal components are:

1. 1 - HTFPGA – Honeywell Part Number 22027498
2. 1 – HT28C256 32kx8 EEPROM – Honeywell Part Number 2203092

   [For the remainder of this report "HTEEPROM" will be used to refer to the HT28C256 32kx8 EEPROM.]

3. 1 - HT6526 32kx8 SRAM – Honeywell Part Number 22019256
4. 2 - 0.1uf power supply decoupling capacitors – Novacap 1210H104M250PH or equivalent
5. 7 – 10nf charge pump capacitors – Novacap 0805H103M500PH or equivalent

A general overview of the architecture and I/O is provided within Section 2 of the Objectives specification (Reference 3). An updated functional block diagram is shown in Figure 1. RPDA package pins and their internal connections are shown in Table 3.

Table 3- RPDA Package Pin Functions and Internal Connections

Package Pin	Signal Name	HTFPGA Connection	HTFPGA Dual Function	SRAM Connection	HTEEPROM Connection	Function
a1	VDD	VDD		VDD	VDD	Power
a2	VSS	VSS		VSS	VSS	Ground
a3	SR_NOE	IO_204		NOE		HT6256 SRAM Output Enable
a4	SR_NCS	IO_198		NCS		HT6256 SRAM Chip Select
a5	IO_1	IO_1				HTFGPA Programmable I/O
a6	IO_5	IO_5				
a7	IO_11	IO_11				
a8	IO_17	IO_17				
a9	IO_26	IO_26				
a10	IO_33	IO_33				
a11	IO_39	IO_39				
a12	M0	M0				HTFPGA Configuration Control
a13	CLOCK	CLOCK				HTFGPA Core Clock
a14	RESETN	RESETN			POROUTN	HTEEPROM Power-on Reset Out / HTFPGA Reset In
a15	EE_NRFSHRQ	IO_53			NRFSHRQ	HTEEPROM Refresh Request
a16	EE_NRFSHACK	IO_54			NRFSHACK	HTEEPROM Refresh Acknowledge
a17	EE_A2	IO_58			A2	HTEEPROM Parallel Address
a18	EE_A5	IO_62			A5	
a19	EE_A8	IO_66			A8	
a20	VSSA				VSSA	HTEEPROM Analog Ground
a21	VDDA				VDDA	HTEEPROM Analog Power
b1	SR_NWE	IO_184		NWE		HT6256 SRAM Wirte Enable
b2	SR_A8	IO_192		A8		HT6256 SRAM Address
b3	SR_A11	IO_200		A11		
b4	SR_A10	IO_202		A10		
b5	SR_D7	IO_194		D7		HT6256 SRAM Data
b6	IO_7	IO_7				HTFPGA Programmable I/O
b7	IO_13	IO_13				
b8	IO_19	IO_19				
b9	IO_27	IO_27				
b10	IO_35	IO_35				
b11	IO_41	IO_41				
b12	IO_51	IO_51				
b13	M1	M1				HTFPGA Configuration Control
b14	M2	M2				
b15	EE_A1	IO_57	A1		A1	HTEEPROM Parallel Address
b16	EE_A3	IO_60	A3		A3	
b17	EE_A6	IO_64	A6		A6	
b18	EE_A9	IO_68	A9		A9	
b19	EE_A11	IO_70	A11		A11	
b20	EE_A13	IO_73	A13		A13	
b21	EE_D7	IO_89	D7		D7	HTEEPROM Parallel Data
c1	SR_A14	IO_180		A14		HT6256 SRAM Address
c2	SR_A13	IO_188		A13		
c3	SR_A9	IO_196		A9		
c4	SR_D6	IO_190		D6		HT6256 SRAM Data
c5	SR_D5	IO_186		D5		
c6	IO_9	IO_9				HTFPGA Programmable I/O
c7	IO_15	IO_15				
c8	IO_21	IO_21				
c9	IO_29	IO_29				
c10	IO_37	IO_37				
c11	IO_43	IO_43				
c12	IO_45	IO_45				
c13	IO_47	IO_47				
c14	IO_49	IO_49				
c15	EE_A4	IO_61	A4		A4	HTEEPROM Parallel Address
c16	EE_A7	IO_65	A7		A7	
c17	EE_A10	IO_69	A10		A10	
c18	EE_A12	IO_72	A12		A12	
c19	EE_A14	IO_74	A14		A14	
c20	EE_D6	IO_86	D6		D6	HTEEPROM Parallel Data
c21	TM_VM				TM_VM	HTEEPROM Test Pin
d1	SR_A12	IO_174		A12		HT6256 SRAM Address
d2	SR_A5	IO_162		A5		
d3	SR_D4	IO_182		D4		HT6256 SRAM Data
d4	SR_D3	IO_178		D3		
d5	IO_145	IO_145				HTFPGA Programmable I/O
d6	IO_137	IO_137				
d7	IO_129	IO_129				
d8	IO_23	IO_23				
d9	IO_31	IO_31				
d10	IO_109	IO_109				
d11	IO_101	IO_101				
d12	IO_100	IO_100				

Table 3 - RPDA Package Pin Functions and Internal Connections (continued)

Package Pin	Signal Name	HTFPGA Connection	HTFPGA Dual Function	SRAM Connection	HTEEPROM Connection	Function
d13	IO_90	IO_90	TESTCLK			HTFPGA Programmable I/O (HTFPGA Test Clock)
d14	EE_A0	IO_56	A0		A0	HTEEPROM Parallel Address
d15	TM_NRFSHOSC				TM_NRFSHOSC	HTEEPROM Test Pin
d16	TM_NRFSHDIV				TM_NRFSHDIV	
d17	TM_NSELALL				TM_NSELALL	
d18	TM_NSELHLF				TM_NSELHLF	
d19	TM_NPOE				TM_NPOE	
d20	TMPDIODE				TMPDIODE	
d21	TM_ECC_NDISABLE				TM_ECC_NDISABLE	
e1	SR_A7	IO_170		A7		HT6256 SRAM Address
e2	SR_A3	IO_154		A3		
e3	SR_D2	IO_176		D2		HT6256 SRAM Data
e4	SR_D1	IO_172		D1		
e5	IO_147	IO_147				HTFPGA Programmable I/O
e6	IO_139	IO_139				
e7	IO_131	IO_131				
e8	IO_123	IO_123				
e9	IO_117	IO_117				
e10	IO_111	IO_111				
e11	IO_103	IO_103				
e12	IO_98	IO_98				
e13	IO_92	IO_92	CENCFG			HTFPGA Configuration Control
e14	EE_CSN	IO_77	A16		CSN	HTEEPROM Chip Select
e15	EE_D0	IO_80	D0		D0	HTEEPROM Parallel Data
e16	EE_D1	IO_81	D1		D1	
e17	EE_D2	IO_82	D2		D2	
e18	EE_D3	IO_84	D3		D3	
e19	EE_D4	IO_85	D4		D4	
e20	EE_D5	IO_86	D5		D5	
e21	TM_VP				TM_VP	HTEEPROM Test Pin
f1	SR_A6	IO_166		A6		HT6256 SRAM Address
f2	SR_A4	IO_158		A4		
f3	SR_D0	IO_168		D0		HT6256 SRAM Data
f4	SR_A0	IO_164		A0		
f5	IO_149	IO_149				HTFPGA Programmable I/O
f6	IO_141	IO_141				
f7	IO_133	IO_133				
f8	IO_125	IO_125				
f9	IO_119	IO_119				
f10	IO_113	IO_113				
f11	IO_105	IO_105				
f12	CSOUT	IO_94	CSOUT			HTFPGA Configuration Control
f13	EE_CFG_PROT				CFG_PROT	HTEEPROM Configuration Protect Pin
f14	EE_WEN	IO_75			WEN	HTEEPRM Write Enable
f15	EE_SELSNP				SELSNP	HTEERPOM Parallel/Serial Configuration Control
f16	EE_SI				SI	HTEEPROM Serial Input
f17	EE_HOLDN				HOLDN	HTEEPROM Serial Hold Pin
f18	EE_SBP1				SBP1	HTEEPROM Block Protect Pin
f19	CHECKN	IO_93	CHECKN		CHECKN	HTFPGA Configuration Control
f20	CONN	CONN			CONN	HTFPGA Configuration Control
f21	POROUTN	POROUTN			PORINN	HTFPGA Power-on Reset Out / HTEEPROM Reset In
g1	VDD	VDD		VDD	VDD	Power
g2	VSS	VSS		VSS	VSS	Ground
g3	SR_A1	IO_150		A1		HT6256 SRAM Address
g4	SR_A2	IO_156		A2		
g5	IO_151	IO_151				HTFPGA Programmable I/O
g6	IO_143	IO_143				
g7	IO_135	IO_135				
g8	IO_127	IO_127				
g9	IO_121	IO_121				
g10	IO_115	IO_115				
g11	IO_107	IO_107				
g12	UNRSTN	UNRSTN				Auxilliary HTFPGA Reset
g13	EE_OEN	IO_76	A15		OEN	HTEEPROM Output Enable
g14	ERRN	IO_78	ERRN		ERRN	HTFPGA Configuration Control
g15	EE_SCK				SCK	HTEEPROM Serial Clock
g16	EE_WPN				WPN	HTEEROM Serial Write Protect Pin
g17	EE_SBP0				SBP0	HTEEPROM Block Protect Pin
g18	EE_SO				SO	HTEEPROM Serial Data Out
g19	CCLK	CCLK			CCLK	HTFPGA Configuration Clock
g20	VSS	VSS		VSS	VSS	Ground
g21	VDD	VDD		VDD	VDD	Power

4.2.2 Number of Gates and Memory Capacity

The HTEEPROM within the RPDA contains 32K words (8-bits each) of memory (256Kbits of total capacity. The HTEEPROM is intended to store configuration data that is used to program the HTFPGA. The HTFPGA configuration file can use up to 16,394 words of this capacity. The remaining memory (at least 16,374 words) is available for other non-volatile data storage.

The HTFPGA has equivalent capacity to an Atmel AT6010 component. This provides up to 6400 register elements and/or up to 32,000 equivalent gates of logic. The number of useable gates is dependent upon the application, complexity of the signal routing, and the synthesis process (i.e., the process by which a behavioral design is translated into a gate-level structural design).

The HT6256 SRAM contains 32K words (8-bits each) of static random-access memory that is 100% available for application memory.

The HTFPGA may access additional memory by dedicating pins to enable memory devices external to the MCM. This is described in the Objectives Specification.

4.2.3 Clocking and Clock Distribution Considerations

Depending on the application (i.e., the HTFPGA configuration), any of the RPDA programmable I/O can be used as a clock pin. Dedicated clocking pins within the RPDA MCM are:

1. CLOCK: HTFPGA core clock (pin A13). This is a centrally distributed clock pin. Using this pin as the primary clocking input to the FPGA will minimize clock skew between for synchronously clocked registers and logic on the HTFPGA.
2. CCLK: HTFPGA configuration clock (pin G19). This pin is an input or an output depending on the HTFPGA mode control (see reference 7). This clock is dedicated for use during the process of HTFPGA configuration only.
3. EE_SCK: HTEEPROM Serial Port Interface clock (pin G15). This pin is used to clock data to and form the HTEEPROM when the serial interface is enabled.

Access between the memory components (HTEEPROM and HT6256 SRAM) and the HTFPGA is asynchronous. Depending on the application, clocking and data access timing considerations (synchronous and asynchronous delays, skew, clock buffering, etc.) could all be issues requiring analysis. These issues can all be analyzed using the Atmel Figaro tool IDS7.6.

4.2.4 High and Low Voltage Requirements

The design is specified for operation at 5V plus/minus 5%. This is consistent with the delay modeling that was used in the development of the HTFPGA timing libraries, and in the design of the HTEEPROM. The HT6256 SRAM is specified for operation at 5V plus/minus 10%. The HTEEPROM also makes use of high-voltage supplies generated internally while writing data to the non-volatile memory cells embedded within it. These voltages (+8.5V and -8.5V) are applied only to the HTEEPROM and it's associated charge pump capacitors. For test purposes only these supply rails are also brought out to RPDA package pins (pins e21 and c21). The HTEEPROM is specifically designed to handle these non-standard voltages.

All capacitors will be procured to a voltage rating so as to insure at least 2x margin to their respective operating voltages.

4.2.5 Functional Simulation and Analysis

Several tools have been used in the pre-configured simulation and analysis of the RPDA, (focusing especially on the HTFGA). These include:

- Schematic Capture and Simulation Tools:
  - Mentor DA en 2002: HTPFGA Schematic capture
  - QSimPro 2004SP5: HTPGA QuickPart (gate/transistor level) simulation
  - Modelsim 5.8d: HTFPGA QuickPart (gate/transistor level) simulation
  - Modelsim 6.1e – HTPGA and RPDA Hardware Description Language (HDL) simulation
- Synthesis and Routing Tools:
  - Mentor Leonardo Spectrum 2006b.12: Gate-level structural synthesis
  - Atmel Figaro IDS7.6.7: Place and route and timing analysis; used with a software patch specific to the HTFPGA (AT6010HLV-010QM)

HTFPGA gate level simulation has been completed using production functional test vector sets and simulated using min/max timing parameters annotated to the netlist via Standard Delay Format (SDF) timing files. The HTFPGA simulation viewpoint in these cases consists of the gate-level representation of the physical structure (i.e., corresponding to the transistor-level physical structure of the HTFPGA rather than a synthesized gate-level netlist representative of a “configured” HTFGPA). A primary objective of this level of detailed simulation is to verify that the HTFPGA can be configured in multiple modes and perform as intended after configuration. These test cases included boot-up and reset simulation in configuration mode 5 (autonomous configuration) and mode 1 (address count-up, external configuration clock) followed by functional testing of configured behavior.

In addition boot-up and reset simulations were completed for mode 2 operation (address count-down, external configuration clock). No post-configuration functional simulation was performed in the case of the mode 2 test case. Simulation test benches were also generated to verify the self-checking functions associated with HTFPGA configuration.

In addition to the gate-level structural simulations Register-transfer-level (RTL) simulations were performed at the top-level of the RPDA to verify correct connectivity between the HTFPGA / HTEEPROM and the HTFPGA / HT6256 SRAM.

4.2.6 Input and Output Characteristics

Internal connections between RPDA components will see capacitive loading of approximately 3.5pF/cm of interconnect routing, plus die pad loading estimated at 4.0pF to 5.0pF. Die pad loading is estimated based on the Honeywell’s HT2000 gate-array I/O models. This is reasonable since these I/O structures are substantially replicated in both the HTFPGA and the HTEEPROM I/O cells. This gives a range of internal loading conditions ranging from approx. 6pf for a single-ended short trace to approx. 20pF for a double-ended long trace. This level of capacitive loading is within standard ranges for these I/O designs.

Except in unusual circumstances, RPDA outputs to external components will be driven by the HTFPGA I/O. When configured as "high-drive" outputs these I/O will have capability to drive up to 105pF of external load (in addition to worst-case internal loading). This will be sufficient to drive other board-level components as well as automated tester interfaces.

Due to similarity to Honeywell HT2000 gate array I/O, the HT2000 Data Book (Reference 8) can be used to estimate rise/fall times (edge rates). Similarly the HT2000 Data Book can be used to analyze transient effect from simultaneous switching outputs where High-drive outputs are equivalent to "15mA" drivers and Low-drive outputs are equivalent to "6mA" drivers.

The HTFPGA uses configurable pull-ups. HTFPGA I/O default configuration is all I/O programmed as pull-up. The HTEEPROM uses a number of hardwired pull-ups and pull-downs for test-mode pins. Details are documented in the respective Honeywell internal product specifications for each integrated circuit.

4.2.7 Power-up Behavior

Power-up response in the case of the RPDA includes HTFPGA re-boot (internal configuration memory initialization) followed by configuration down-load. The primary mode of configuration is Mode 5 (autonomous configuration via the HTEEPROM using the HTFPGA CCLK). This mode of configuration is supported by the HTEEPROM design which incorporates customized HTFPGA configuration interface. RPDA simulations of the HTFPGA / HTEEPROM power-up sequence revealed a design flaw in this interface. Essentially the HTEEPROM did not respond at the required time (2 clock cycles after the HTFPGA boot-up sequence was completed) in order for the HTFPGA to "see" the HTEEPROM and start the down-load sequence. This was corrected by an inter-connect change that was applied to the initial HTEEPROM design verification wafers. The change involved modifying the third-layer metal interconnect layer and could be applied toward the end of the wafer-process sequence. This made it possible to salvage the wafer lot that was in progress. Overall this delayed the completion of the initial HTEEPROM wafers by about a month. Part of this delay included simulating the modified design to verify correct power-up and configuration behavior.

4.2.8 AC Performance Considerations

Automated static timing analysis is not currently possible at the MCM level. However, as long as write enable, address, and data to and from the memory components are registered at 10MHz or less, then set-up and hold requirements will be met.

During autonomous configuration load HTEEPROM access to/from the HTFPGA is synchronized to a configuration clock (CCLK, nominally 1MHz) generated within the HTPFGA.

Other AC performance considerations (propagation delay, maximum output loading, timing margin, etc.) are dependent upon configuration and would normally be analyzed by Atmel Figaro timing analysis.

4.2.9 Power Consumption and Power Dissipation Considerations

Analysis of power consumption has been included within the Objectives Specification (Reference 3). Power consumption is strongly dependent on configuration. The targeted demonstration configuration clocked at 1MHz power dissipation is on the order of 100mW. A more worst-case situation with 100 I/O each driving 80pF at 5MHz

would have power dissipation on the order of 1W. This power dissipation would be localized primarily within the HTPGA. The thermal characteristics of the MCM package should result in only a few degrees centigrade of temperature increase from the die to the package case. The design specifications allow for up to 25 degrees centigrade of internal temperature increase (T_{Case}=225°C, $T_{Junction}$=250°C).

4.2.10 Proximity, Matching and Routing Considerations

There are no significant internal sensitivities of the RPDA design from a signal cross-talk or signal routing consideration. MCM signals will be routed within a plane at 5 mil spacing or separated from other signals by power/ground planes. Maximum coupling between digital signals at 3.5pF/cm of routing trace would be 10pF which is not considered to be an issue. Power/Ground routing within the MCM will be accomplished by dedicated power/ground planes, so that there will be no significant internal power/ground voltage drops. Package pins are arranged on 100mil centers. Normal board routing procedures will be applicable without issues.

4.3 Test Considerations

4.3.1 Hardware Design for Test Features

No special test circuits are necessary. The RPDA pin-out and functional architecture along with test features built into the individual components result in a highly controllable and observable structure.

All of the signal routes connecting internal components are brought out to RPDA package pins (except for HTEEPROM charge-pump capacitors). All of the internal devices can have their outputs tri-stated (i.e., put into a high-impedance state) so that each internal component can be individually tested in situ. The HTFPGA can be configured as a direct port to the HT6256 SRAM and/or the HTEEPROM to directly test chip-to-chip connectivity. The HTFPGA can be configured as an XOR tree and output tree to directly measure DC I/O parameters. HTEEPROM test pins are brought out to monitor Error Correction features, test the memory refresh timer, and enable global memory and block writing. A temperature-dependent diode on the HTEEPROM is bonded out to enable characterization of internal temperature rise.

Configuration data can be loaded directly into the HTFPGA via external interfaces for manufacturing test purposes. Configuration data can also be loaded into the HTEEPROM either through the HTEEPROM parallel interface or the HTEEPROM serial interface.

All of the HTFPGA I/O DC parametric testing is envisioned as a functional state machine that sequences through a standard set of tests. For example:

1. Configure all I/O as inputs except one that is configured as an output; inputs connected to the output via an AND tree. Test input logic levels (VIH/L)
2. Configure all I/O tri-stated outputs. Measure stand-by current and High-impedance output currents (IDDSB,IOZ)
3. Configure I/O with one input, remainder connected via a serial scan register. Measure output logic levels (VOH/VOL)
4. Configure HTFPGA as a direct “pass through” port to the SRAM. Verify interconnect to/from SRAM by read/write via the HTPGA port.

5. Configure HTFPGA as a direct "pass through" port to the HTEEPROM. Verify interconnect to/from HTEEPROM by read/write via the HTPGA port.

A sequence of this nature may become a standard functional screen for all RPDA hardware. Other means of interconnect testing may also be envisioned.

4.3.2 Fault-coverage Considerations

It is assumed that sufficient fault coverage of individual components will be provided by wafer-level testing prior to assembly within the RPDA. Fault coverage for individual components is expected at 99% or more. Note that hot-chuck wafer-probing by automated testers is limited to 200°C.

By the above strategy, RPDA fault coverage objectives would be primarily focused on detecting wirebond and package-level interconnect failures. Gross handling/assembly damage would be observed during interconnect testing.

4.3.3 Configuring and Post-Configuration Testing of the RPDA

A general process for RPDA general testing, configuration and screening may be as follows:

1. Power-up the RPDA, hold the CONN (configuration control) pin low to prevent autonomous configuration.
2. Using the serial interface, load the HTEEPROM with data to configure the HTFPGA for DC I/O parametric testing (as described in 3.2.1 above).
3. Cycle power (which will result in configuring the HTFPGA).
4. Run functional stimulus and perform DC parametric tests.
5. Using the serial interface, load the HTEEPROM with data to configure the HTFPGA for wirebond and package interconnect testing (as described in 3.2.1 above)
6. Cycle power (which will result in configuring the HTFPGA).
7. Run functional stimulus for interconnect / wirebond tests. After this point the RPDA could be sold and delivered in an "un-configured" format.
8. Using the serial interface, load the HTEEPROM with data to configure the HTFPGA for the end-user application.
9. Cycle power (which will result in configuring the HTFPGA).
10. Run functional stimulus to test the configured design. After this point the PRDA could be sold and delivered in its configured format.
11. OPTION: Using the serial interface, load the HTEEPROM with data to configure the HTFPGA for burn-in configuration. NOTE that burn-in configuration could be the same as the end-user configuration, or optimized to the end-user configuration. Also, a burn-in configuration could be developed for an "un-configured" format deliverable.
12. Cycle power (which will result in configuring the HTFPGA).
13. Run functional stimulus for burn-in test. Burn-in test configuration may also be applied for extended life test.

Finalization of the procedures for test, screening, and life-test will be achieved and implemented as part of the Phase 2 program activity.

Note that the above sequence could result in writing up to half of the HTEEPROM (for configuration purposes) at least four times. This is in addition to the number of HTEEPROM write cycles required for comprehensive wafer-level testing prior to assembly within the RPDA. The durability of the HTEEPROM over multiple write operations is currently being investigated (as an independently funded activity parallel to this project). The outcome of this investigation may limit the number of available HTEEPROM write cycles, and thereby impact this plan. Results of this testing will be available by the end of the September, 2007.

4.4 Multi-chip Module Package Design and Construction

The MCM package design is based on concepts and materials successfully employed on other high-temperature MCM components developed by Honeywell.

4.4.1 Components, Bill of Materials, Configuration Management

Major components and sources of supply for the complete manufacture of the MCM have been preliminarily established. In addition to the IC components, this includes the ceramic package and lid, chip capacitors, adhesives for die and capacitor attach, bond-wire, and marking ink. These listed on a preliminary bill of materials which also lists operating procedures and processes used during assembly.

4.4.2 Physical Dimensions, I/O Assignment and Location

Overall package physical dimensions are shown in Figure 2. Figure 3 shows the package pin arrangement and location. Signal assignment to the package pins is also defined in Table 3.

4.4.3 Component Floor-plans and Wire-bonding

Details of component pad locations and wire-bonding are shown in Figure 4. These have been reviewed by Honeywell assembly process engineers for compatibility with Honeywell's wire-bond assembly equipment and procedures. Die maps and bond-pad assignments for integrated circuits are defined within the design database maintained by Honeywell for each die type

4.4.4 MCM Technology and Materials, and Vendor Selection

The MCM materials and assembly technology are based on prior successful experience with high-temperature. Proven materials and processes include:

Package Type:	High Temperature Co-fired Ceramic MCM
Package Body:	90% Al_2O_3 Multi-layer
Internal Metallization:	Tungsten
Pins, Seal Ring, Lid:	Kovar (Fe-Ni-Co)
External Metal (Plating)	Gold (80µin.) over Ni
Die Attach:	Organic Cyanate Ester
Wirebond:	Ultrasonic Al wedge Bond
Hermetic Seal:	Welded Kovar Lid

4.4.5 Die Bond Options

As shown above, the planned die attach method employs an organic cyanate ester conductive adhesive. However, gold-eutectic die bonding is also an option. Electrically conductive die bonding will be employed to ensure that the die backside is at a known electrical potential. All die bond surfaces within the package will be electrically connected to VSS (ground).

4.4.6 MCM Layers

The MCM layers are shown in Figure 5. There are three power/ground planes and three signal routing layers.

4.4.7 Package Routing, and Final Design Acceptance

Layout of the signal layers and associated vias will be performed by the MCM package vendor. Routing, and verification to the netlist supplied by Honeywell, is an automated process. Honeywell will receive final artwork for review and approval at the end of Phase 1.

4.5 Multi-chip Module Performance Characteristics

4.5.1 Internal Signal and Power Routing Considerations

Digital VDD and VSS for all three active components are brought in through 3 pairs of pins and routed using the power/ground planes. There are two 0.1uF supply de-coupling capacitors within the package.

Analog VDDA and VSSA are routed separately to the HTEEPROM to power charge-pumps used to create high voltage supplies used for writing to the HTEEPROM. These are very low current draw (10uA) and do not require special routing.

Signals will be routed within the signal-routing layers using 5-mil wide traces with 5-mil spacing. Long routes and cross-overs are minimized by placement of the HTFPGA between the HTEERPOM and HT6256 SRAM, and by the intentional design of the HTEEPROM placing signals that are used with the HTFPGA on the side of the HTEEPROM die that is adjacent to the HTFPGA.

4.5.2 I/O Electrical Characteristics

At the frequencies and power-dissipation levels anticipated for this design, it is expected that I/O characteristics will be primarily determined by the internal components rather than by the package design.

4.5.3 Thermal and Mechanical Performance Considerations

The MCM materials and sealing process are capable for temperatures in excess of 300°C. Die-bond and capacitor attach adhesives have been used in similar package applications with an adhesive curing temperature of 300°C and burn-in and life testing at 250°C. Residual Gas Analysis (RGA) of previous package designs demonstrates that adhesives pass requirements of less than 5000 PPM after 1000 hour life test. These adhesives have been qualified both for high-temperature use as well as for military and space applications.

Thermal conductivity of the package materials should result in internal self-heating of less than 5°C/W (junction to case).

Shock and vibration testing is not within the scope of this program, and in general is very difficult to perform at temperature. However, similar package materials and

assembly processes have been successfully employed in hih shock and vibration applications. Shock and vibration characteristics of the target environment have been noted in the Objectives Specification[1] and the consensus is that these are likely to be achieved by this package. Resonant frequency of the package and sub-components (including lid and internal bond-wires) should be well above the frequencies cited in the Objectives Specification. The rigidity and strength of the co-fired ceramic body and attached Kovar seal ring, and high-performance adhesives will provide capability to handle a high-shock environment.

4.6 MCM Component Assembly Process and Requirements

Assembly materials and processes have generally been proven on prior designs. Other than interim and final electrical test procedures, there are no new assembly processes to be developed. A preliminary assembly process flow has been compiled citing 25 pre-existing documented operating procedures. Prior experience with specific materials, components and/or sub-processes includes:

- Seam sealed lid
  - No issues with high temperature operation or storage
- Adhesives
  - Mechanical (non-conductive) adhesive: Previously used on product cured at 300°C and burned in at 250°C – used for "staking" capacitors.
  - Die-bond and Capacitor Termination (conductive) adhesive: Previously used on product cured at 300°C and burned in at 250°C
  - Both adhesives qualified for military and space products
  - RGA analysis of previous package designs demonstrates adhesives pass RGA with values less than 5000 PPM after life test.
- Package
  - 147 pin Alumina – no issues with high temperature burn-in or storage. Previous packages from the same vendor and similar design have shown no issues with use at high temperature.
- Die
  - Fabricated using Honeywell's High Temperature wafer fab process
- Capacitors
  - Planning to use capacitors rated to 250°C, 20% tolerance

Additional assumptions and/or considerations for the RPDA assembly process include:

- Adhesive component attach
  - Auto dispense of adhesives
  - 300°C cure
- Manual die and capacitor placement into adhesives
  - Standard automatic wire bonding, same wire as used on previous high temp product
- Electro-static Disharge (ESD) Considerations
  - Die have been designed for class 2 – greater than 2000V input protection
- Constant acceleration

[1] The hardware is intended to meet the conditions outlined in paragraph 7.1 (Oil and Natural Gas Wells) of AIR5711, "High Temperature Electronic Component Testing" Draft standard of the SAE AE-7 Sub-committee, 11-27-2006

    - Die attach has been shown to withstand 30000G constant acceleration without damage in both Y1 and Y2 orientation
    - Wire bonds unaffected by 30000G constant acceleration
- Leak Test
    - He pressure bomb – similar package demonstrated capability to withstand 5 atmosphere without leakage or adverse effects
- X-Ray analysis of seam seal and die attach would be problematical due to the distribution of pins on the underside of the package.

4.7 MCM Tester Considerations

4.7.1 Tester Compatibility, Test Equipment and Fixturing

It is expected that evaluation and production screening will make use of automated test equipment that was previously installed and is in use at Honeywell's facility in Plymouth, Minnesota. Multiple test platforms are available. These have been assessed relative to the RPDA requirements for tester I/O capacity, stimulus and measurement capability, and compatibility of test fixtures with the RPDA package. The test platform that Honeywell intends to use has capacity for 139 signal pins with bi-directional force/measurement capability, and is physically compatible with a test fixture incorporating a 21 x 21 pin-grid array socket with pins on 100 mil centers. High-temperature sockets have been identified which can be configured for the RPDA package using high-temperature pins. A custom motherboard will need to be developed, of similar complexity to Honeywell production gate-array test interfaces.

One limitation of current automated test environment at Honeywell is that maximum test temperature is limited by test equipment that can supply a stream of air (applied to the part under test) that is heated to 225°C. Due to thermal conduction through the package pins, cabling, and test board this will not result in achieving an internal die temperature of 225°C. The RPDA can be feasibly exercised in ovens (as in burn-in) at temperature up to 250°C. However, in the oven environment only limited test capability is available. An alternative that may be feasible is to develop a conductive heater for evaluation testing that would rest on the package lid during test (rather than applying heat via the 225°C air stream). Feasibility of this approach will be investigated and potentially implemented during Phase 2 of the program.

Burn-in and life-test boards will be developed in Phase 2 using high temperature components and materials. Definition of a dynamic burn-in configuration that uses minimal external stimulus will be a goal of Phase 2 development.

4.8 Reliability Considerations

Reliability considerations include inter-connect electro-migration, Electro-static Discharge (ESD) withstand capability, and HTEEPROM data retention and durability with data cycling.

For the RPDA design, the worst-case for electro-migration is associated with output loading for the HTFPGA I/O. The HTFPGA I/O structures are based on HT2000 gate array I/O that have proven reliability and have established loading guidelines for electro-migration. Analysis projects that maximum capacitive output load at 11.6MHz switching rate (100% duty cycle) is 125pF. This should be sufficient for the intended applications.

ESD withstand capability is likewise expected to meet requirements (2000V using Human-body Model for ESD discharge). This is based on prior assessment in the case of the

HT6256 SRAM, and on the basis of similarity to HT2000 gate-array I/O structures (with associated ESD protection networks) in the case of the HTEEPROM and HTFPGA.

HTEEPROM data retention will be inherently exercised by life testing that will be conducted in Phase 2. In addition HTEEPROM data retention and data cycling will be assessed by parallel activity under separate funding.

4.9 Demonstration Configuration (Multi-Channel Data Acquisition Controller)

Demonstration of the programmability of the RPDA and feasibility for use in down-hole Data-acquisition applications is a major objective of this program. A significant effort is therefore devoted to the development of a targeted functionality that can be embedded in the RPDA. **A preliminary specification for this demonstration configuration, and it's application in a down-hole data acquisition scenario, is provided as the appendix, "*Multi-Channel Data Acquisition Controller Design Specification*".** This functionality has been defined as behavioral VHDL code and simulated using an Register-Transfer-Level (RTL) simulation. The behavioral code has been synthesized to a gate-level structural implementation. It has been verified that this design will fit within the HTFPGA and can be successfully routed.

The Multi-Channel Data Acquisition Controller (MCDAC) design specification forms the basis for development of test procedures for the demonstration configuration. The MCDAC design will be reviewed and finalized by the end of Phase 1 so that test development can be completed during Phase 2.

5.0 Updated Risk Discussion

The top five program risks as captured in the Objective Specification (January 2007) were identified as:

1) Inter-operability of the system components;
2) Test development costs over budget;
3) Incomplete test coverage;
4) Failure to develop a life-test configuration that sufficiently exercises/stresses the hardware;
5) HTFPGA configuration issues, especially problems using design tools.

At this point in the program these items are substantially resolved. Risk item number 1 has been significantly reduced by the Phase 1 activity to date. A high-fidelity Verilog simulation database representing the detailed physical implementation of the HTFPGA has been developed. This has been verified by comparison of HTFPGA simulated stimulus/response to hardware test stimulus/response patterns. Employing this design viewpoint in top-level simulations of the RPDA has in fact revealed inter-operability issues between the HTEEPROM and the HTFPGA, specifically issues relating to autonomous configuration of the HTFPGA. As a result, corrective action has been taken and the HTEEPROM design has been modified. This has proven the value of the simulation database and reduced the risk of additional issues.

As regards risk item number 5, test specification and development costs have in fact been higher than planned, but for reasons beyond the scope of this program, namely that it was assumed HTEEPROM procedures would be in place from other programs when that has not

been the case. However, significantly lower-than-planned costs associated with MCM package design have enabled additional budget to be applied to the HTEEPROM test development scope.

Risk item number 3 has been reduced to a logistical issue only. The architectural design of the RPDA hardware and subsequent assessment of testability make it clear that the combination of component features and package pin-out provides for a high level of test coverage. If for any reason the program does not achieve a highly comprehensive test, it would merely be due to funding and/or resource issues and not due to an inherent deficiency in the hardware design.

The probability of risk item number 4 becoming an issue is likewise reduced by the current understanding and progress in the Phase 1 design activity.

With respect to risk item number 2, it has indeed been difficult earning to use the Atmel FPGA configuration tools, and in applying them to successfully meet the configuration intent of the Objective Specification. However, these problems are now behind us.

Looking forward there are several new concerns to call attention to:

1) HTEEPROM Functional Performance and Durability: HTEEPROM component development to date has been primarily accomplished under a previous cooperative research agreement between Honeywell and U.S. Department of Energy (DE-FC26-03NT41834). The original intent of that program involved carrying the HTEEPROM development through functional verification, test development, and characterization of durability versus number of write cycles. Therefore it was assumed that HTEEPROM functionality and durability would be proven prior to use in this project. Unfortunately, completion of the HTEEPROM product wafers has been delayed, and therefore functionality and durability has not been demonstrated. To compound the problem, funding under the prior agreement has been used and the period of performance has expired.

   The question of write-cycle durability can be answered without actually testing the HTEEPROM. The limiting factor is gate-oxide wear-out as a factor of applied voltage during write operations and the cumulative time at voltage. This issue can be assessed indirectly by testing gate-oxide test structures independently of completing HTEEPROM functional verification and test procedures. This is being pursued as a separately funded parallel activity and should enable durability assessment by the end of September, 2007. If this study shows that the HTEEPROM has limited write-cycle capability then the usage profile for the application will need to be modified accordingly (i.e., limit the number of times the HTEEPROM can be written).

   The impact of a non-functional HTEEPROM is a greater concern. Wafer-level test procedures are being developed and applied to the HTEEPROM under the assumption that the design is functional, and that these procedures will be substantially re-used for RPDA package-level test. If it turns out that the HTEEPROM is not functional, then root cause analysis will ensue, presumably followed by corrective action that would likely involve a design correction and a new wafer lot.

   It is reasonable to expect that functional assessment (or at least partial assessment) of the HTEEPROM could be completed concurrent with the MCM package build (fourth quarter of 2007). The outcome may have a significant impact on Phase 2 activity and schedule. In the best case, the HTEEPROM will perform as designed. In that case the issue will be limited to the cost and schedule impact for developing test procedures and assessing functionality. In a less fortunate case, the HTEEPROM would require some re-design. In that situation it may be possible for the program to fund a new wafer lot.

This could work, for example, if the program could get by with HTFPGA die obtained from the prior agreement and therefore re-direct funds from HTFPGA fabrication (as currently planned) to 2nd pass HTEEPROM fabrication. In the worst case, it may be that the HTEEPROM cannot be fixed within the funding and/or period of performance for this project. In that scenario, it may still be possible to verify the RPDA package and configured functionality except that HTFPGA configuration would need to be down-loaded from an external source rather than from the HTEEPROM. It would be assumed in that situation that the RPDA development would be completed in parallel with any correction required for the HTEEPROM, and that at the end of the program the way forward to commercialization would remain open.

2) HTFPGA Synthesis and Configuration Tools and Support: Development of HTFPGA configuration files relies upon use of Mentor Leonardo software for synthesis and Atmel Figaro software for place/route and timing analysis. Both of these tools are at or close to the end of their commercial life-cycle at their respective companies. This does not mean that they cannot continue to be applied for future RPDA applications. However it does mean that Mentor and Atmel cannot reasonably be counted on to provide application support. This does not significantly impact the scope of this project, but is does have implications for the longer-term. In particular, Honeywell will likely be required to provide dedicated toolkit and applications support for development of RPDA configurations. This would be true in any case, but the scope of this support is larger than it would be if Atmel and Mentor continue to offer and support these software development tools.

3) New capacitor-attach adhesive introduction in 2008: The adhesive used to secure capacitors within the RPDA package is being discontinued by the manufacturer. Honeywell is in the process of identifying and qualifying an alternative for introduction in 2008. There is a negligible risk from this transition as it regards completing the scope of this cooperative research agreement. However, in the worst case it could affect eventual production (completion of product qualification and/or thermal and mechanical performance). On the other hand, it is also possible that the transition to a new adhesive could be beneficial (i.e., accelerate product qualification and/or improve performance).

4) Availability of high-temperature Pin-Grid-Array sockets: High-temperature sockets are not easy to procure. Occasionally it is necessary to obtain them from “after market” suppliers after production is discontinued. This could impact timing and cost for procurement of sockets needed for test and/or burn-in boards.

6.0 Program Cost and Schedule Forecast

To date program costs is favorable versus plan and schedule is slightly unfavorable versus plan. Un-anticipated costs associated with HTEEPROM test specification and test development have been more than offset by savings in MCM package development. Current status versus schedule is slightly behind plan due to diversions of resource to diagnose and correct the HTEEPROM / HTFPGA configuration interface, and also to some difficulty in applying resources to the un-anticipated HTEEPROM test activity.

Looking forward, if everything proceeds according to plan, the critical path to program completion is MCM fabrication. This is not funded until Phase 2. The Program Management Plan assumed a 12 week vendor cycle time for MCM package fabrication. It is now understood that the vendor cycle time will be 16 weeks.

The most efficient scenario for overall program cost, schedule, and technical performance would be to allow some overlap (approximately 1 month) between the start of Phase 2 tasks (in

particular the MCM procurement) and completion of Phase 1 activity (including HTEEPROM test development and functional verification). It is also reasonable to extend the period of performance for Phase 2 by several months in order to absorb the longer cycle time for package development and also to mitigate against some of the program risks.

7.0 Conclusions

The project objectives are being met. Administrative tasks and report have been completed per the schedule of deliverables. Phase 1 technical tasks are substantially complete. Accomplishments include:

- MCM package design,
- Development preliminary bill or materials and assembly process flows
- RPDA hardware electrical design and analysis
- validation of HTFPGA simulation databases
- Installation and verification of HTFPGA configuration tools and procedures
- Detection (via simulation) of HTEEPROM / HTFPGA configuration issues and corrective action identification
- Top-level simulation including verification of configuration and post-configuration behavior
- Specification, synthesis, and RPDA successfully configured (through the design tool flow) for a Multi-channel Data Acquisition Controller (MCDAC).

The planned program scope to date has been completed at lower cost than planned. Test specification activity has required more effort than planned due to the necessity of completing HTEEPROM test specification and development of test procedures for HTEEROM functional verification.

The biggest risk to the program is the availability of HTEEPROM components with demonstrated functional capability. Even so, successful accomplishment of the project objectives is highly likely.

Figure 1

RPDA Functional Block Diagram

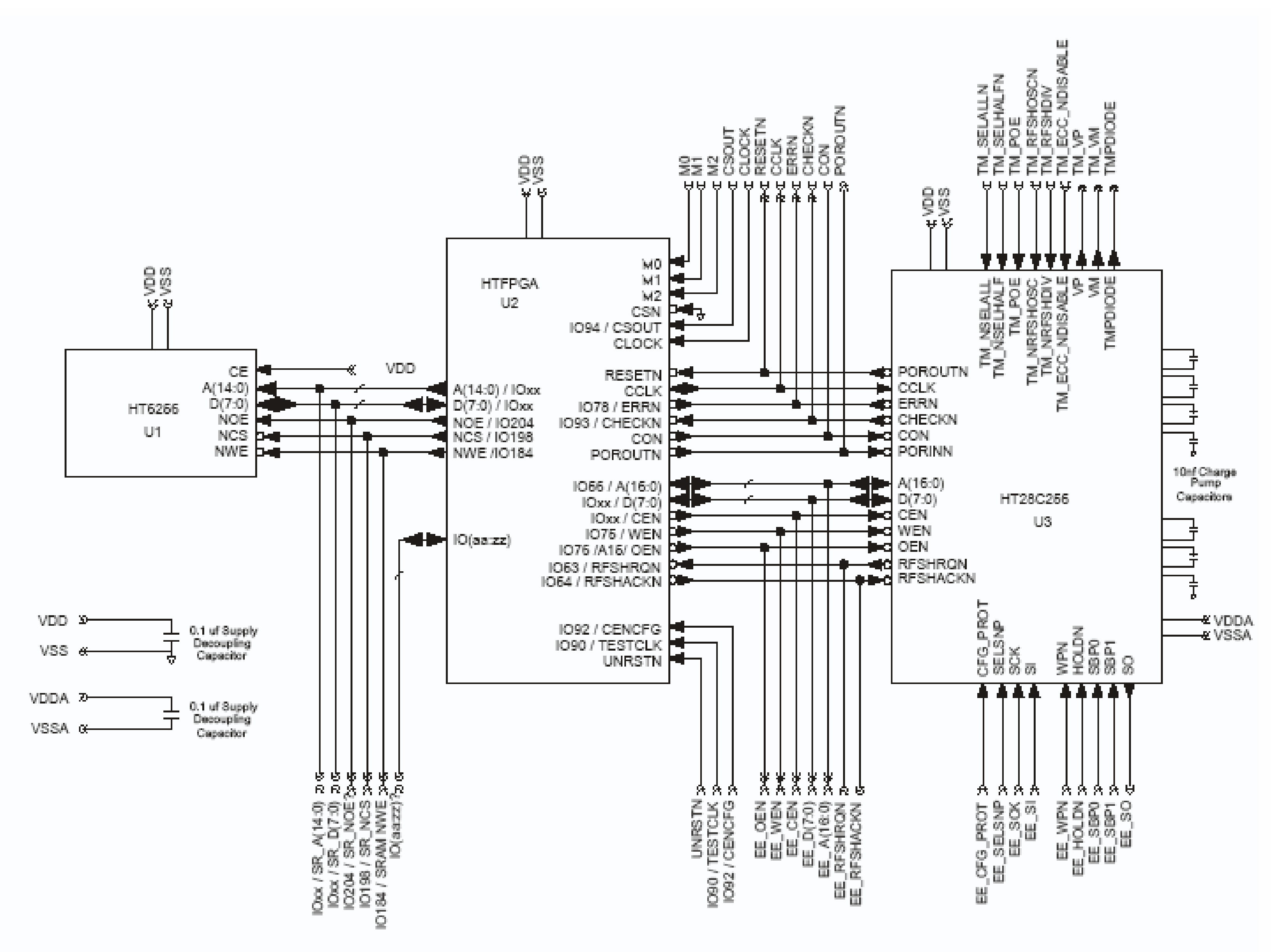
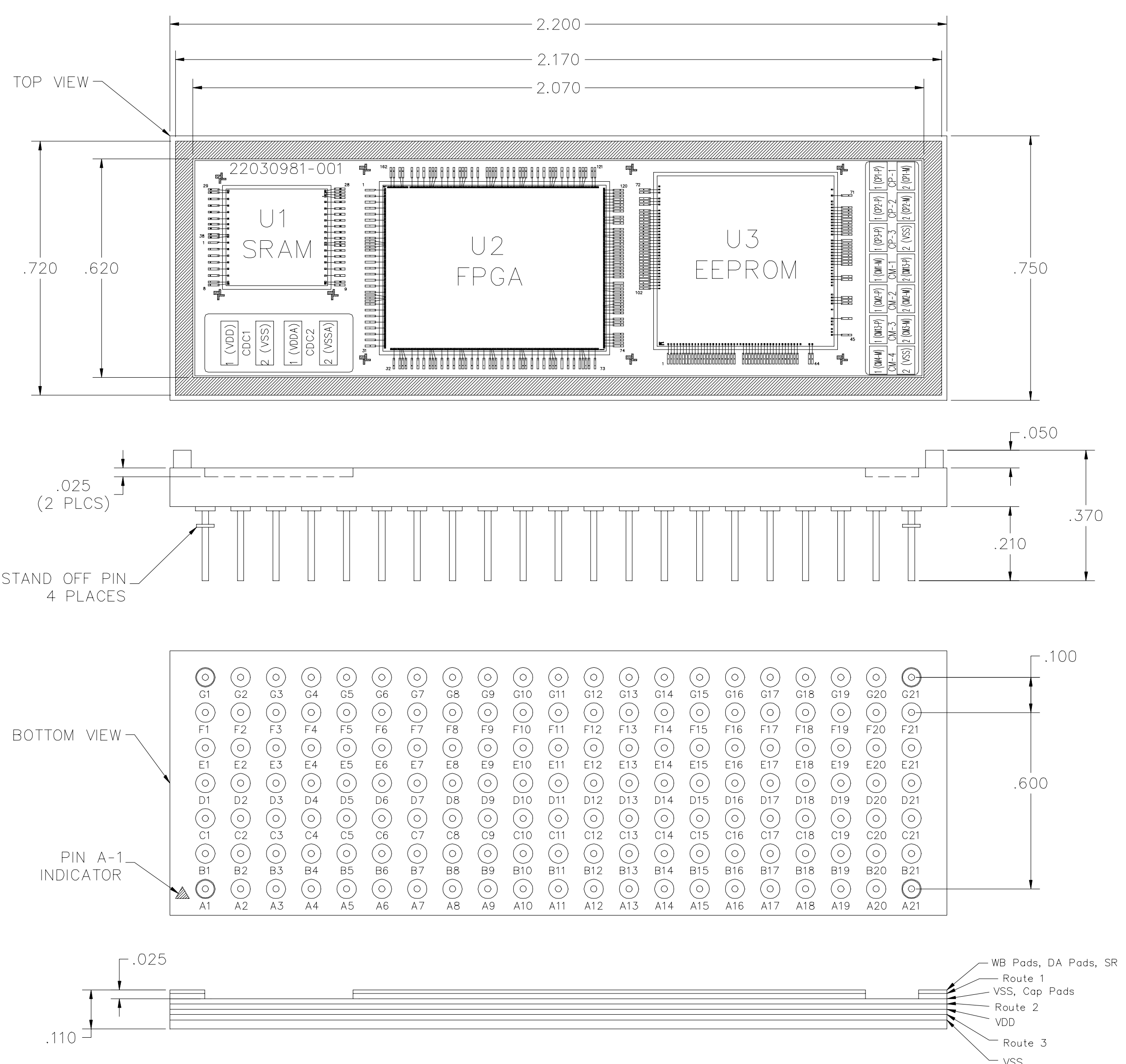


Figure 2

MCM Package Physical Dimensions



CAPACITORS	
CAPACITOR NO.	CAPACITOR TYPE
CDC1	1210
CDC2	1210
CP1	0805
CP2	0805
CP3	0805
CM1	0805
CM2	0805
CM3	0805
CM4	0805

1. PLATING - ELECTROLESS GOLD PLATE 60-225 MICRO-INCHES OVER 50-350 MICRO-INCH ELECTROLESS NICKEL.
2. HONEYWELL SPEC. 22005260 SHALL APPLY UNLESS OTHERWISE SPECIFIED IN PURCHASE ORDER
3. SR, DIE ATTACH PADS, WB TARGETS AND PART NUMBER TO BE TIED TO VSS
4. ELECTRICAL CONTINUITY (SHORTS & OPENS) SHALL BE 100% INSPECTED ON ALL PARTS.

Figure 3: RPDA Pin Locations

Figure 4a

HT6256 SRAM Component Pad Locations and Wire-bonding

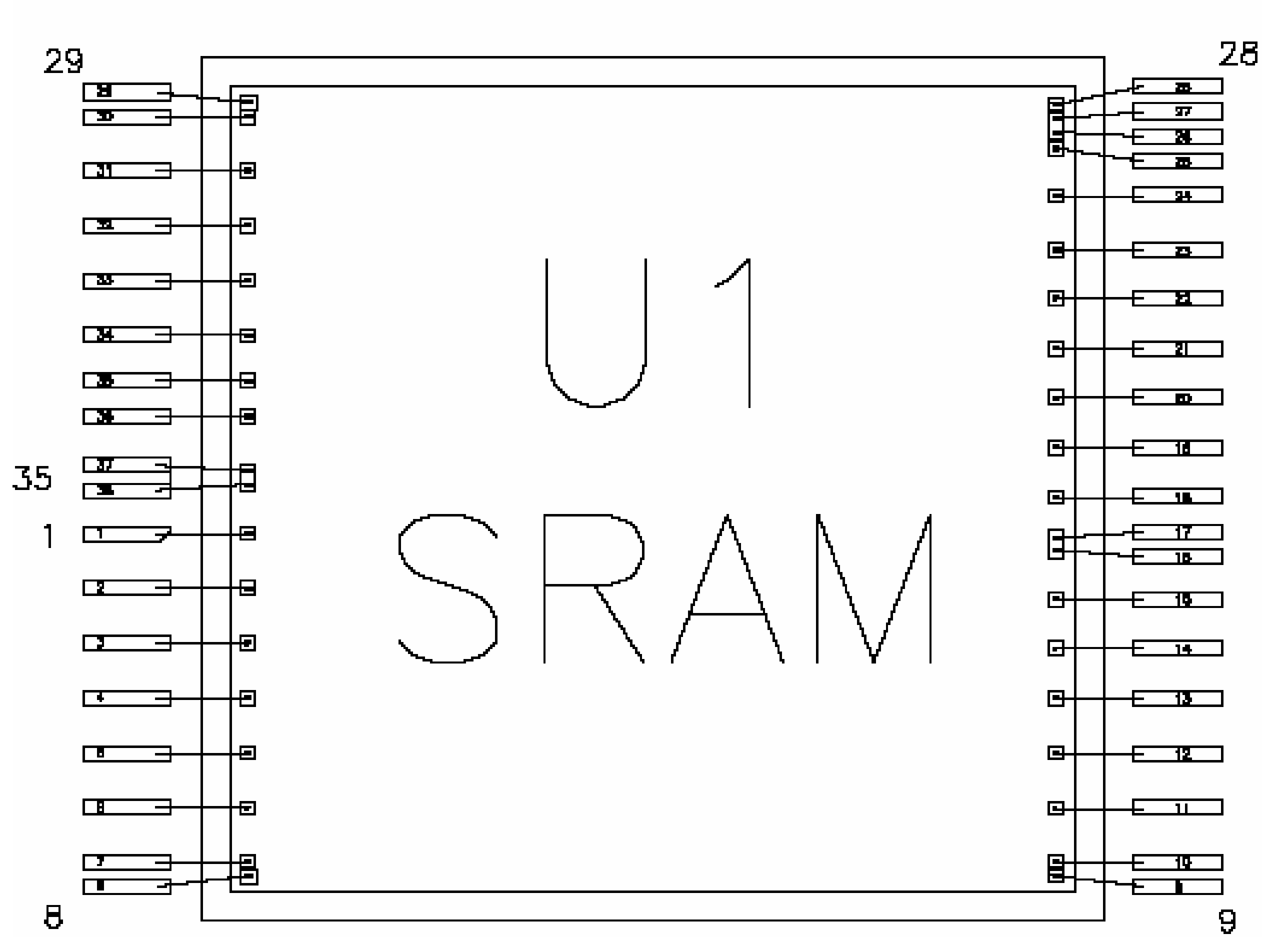


Figure 4c

HTEEPROM Component Pad Locations and Wire-bonding

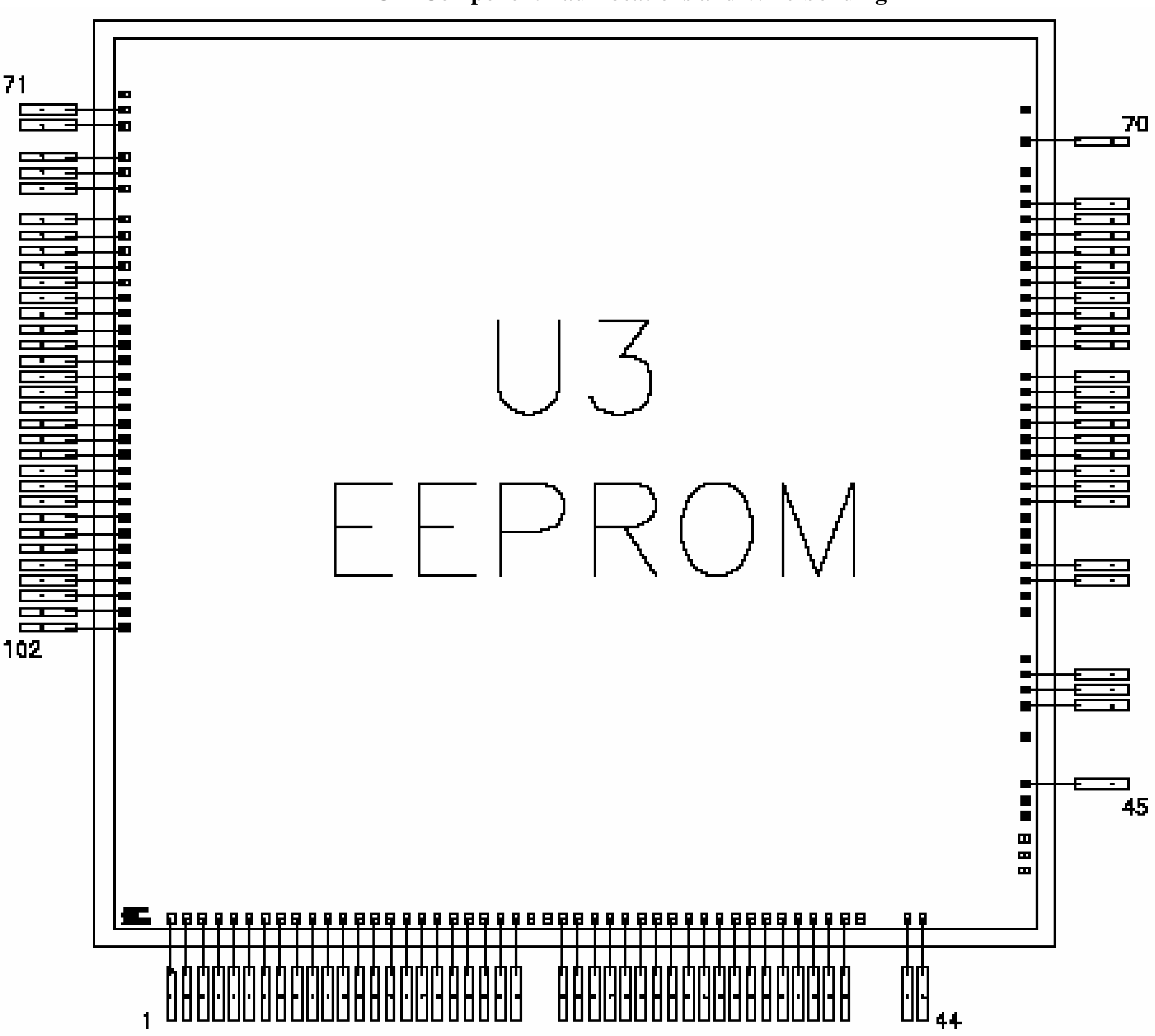


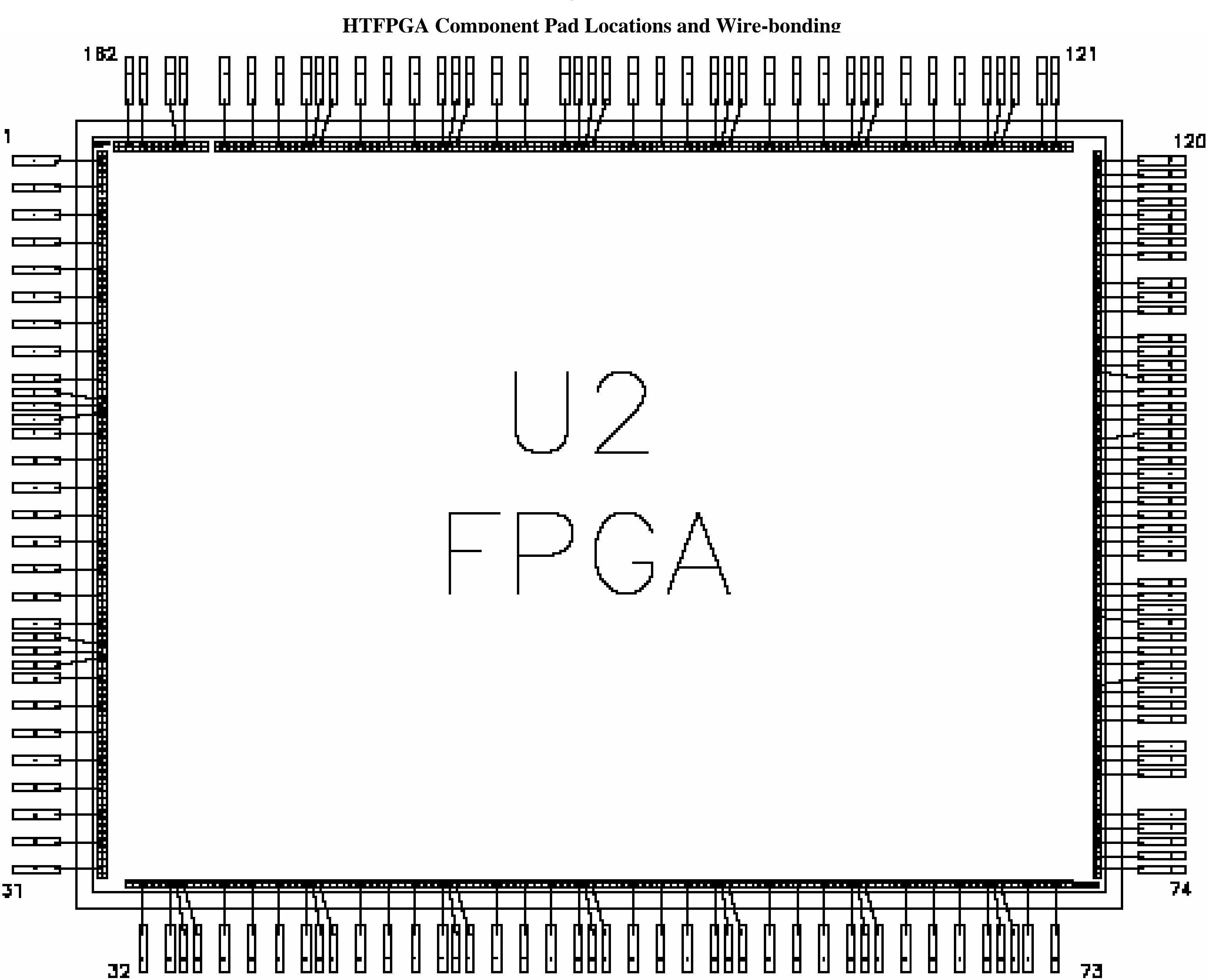
Figure 5

MCM Layers

Kovar Seal Ring, .050"
WB Pads, DA Pads, SR, .010"
Route 1, .015"
VSS, Cap Pads, .015"
Route 2, .015"
VDD, .015"
Route 3, .015"
VSS, .025"
.160
.025
.110

Figure 4b

HTFPGA Component Pad Locations and Wire-bonding



High Temperature Multi-Channel Data Acquisition Controller Design Specification

APPENDIX to

Topical Report - Phase 1 (Final Report of Phase 1)

Deep Trek Re-configurable Processor for Data Acquisition (RPDA)

Revision 1.0
12 October 2007

Author:
Mike Johnson

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1 Introduction

1.1 Overview

This Multi-Channel Data Acquisition Controller (MCDAC) design provides a high temperature module to control and record up to 8-channels of analog data when used in concert with Honeywell's HTADC18 High Temperature 18-bit Analog-to-Digital Converter (ADC) and Honeywell's HT507 High Temperature 8-Channel Analog Multiplexer (AMUX). This design is implemented using the Reconfigurable Processor for Data Acquisition (RPDA).

1.2 Device Description

The MCDAC is built on Honeywell's high temperature Reconfigurable Processor for Data Acquisition (RPDA) platform [1]. This is a multi-chip module (MCM) containing three Honeywell High Temperature products: a field programmable gate array HTFPGA, an HT28C256 EEPROM containing the boot code for the HTFPGA and an HT6256 32Kx8 SRAM. This design is targeted for autonomous and semi-autonomous data logging functions as might be used in deep well measurement while drilling (MWD) and data logging operations.

The MCDAC is organized around a controller/scheduler function that provides data sampling at regular schedules of an external ADC/AMUX combination. Scheduling of measurements is based on programming of external pins. Autonomous measurements occur based on an internal timer derived from the primary SYSCLOCK, which starts the measurement/logging function. Alternatively, measurement on demand can be programmed to occur whenever the SAMPLE_NOW signal is asserted. From one to eight analog channels can be selected for data logging based upon the state of the CHANNEL_SEL bus.

An ADC/AMUX interface function directly controls the external HTADC18 [2], providing wake, measure, and sleep commands through the ADC four-wire Serial Peripheral Interface (SPI) pins, to the HTADC18's 18-bit and 8-bit converters. The ADC/AMUX function also directly controls the address and enable pins of an HT507 [3] analog multiplexer, to steer up to eight channels of analog signals to the front end of the HTADC18.

A First-In/First-Out (FIFO) function is included which takes each 8-bit and 18-bit measurement and stores them along with health and status information into a 32-bit word. Up to 8192 32-bit words can be logged by the on-board memory.

An industry standard SPI interface is used for data transfer to and from the MCDAC at data rates up to 1MHz. The SPI bus is activated through a chip select, enabling communication via the SPI Data In and SPI Data Out pins. Through this interface several operations can occur: the HTADC18 can be put into active and sleep modes, the FIFO data can be downloaded, or most recent measurement data can be downloaded.

2 High Level Description

2.1 Functional Description

The MCDAC is a multi-chip module (MCM) containing a High Temperature Field Programmable Gate Array (HTFPGA), a High Temperature 32Kx8 Static RAM (HTSRAM) and a High Temperature 32Kx8 EEPROM. For this MCDAC design the HTFPGA is configured to control an eight channel High Temperature Analog MUX and an 18-Bit High Temperature Analog-to-Digital Converter. The HTEEPROM is only used as a boot ROM which contains the programming for the HTFPGA. The HTSRAM is used as data storage space in the form of an 8K by 32-bit FIFO. The MCDAC can be programmed through external pin selection to perform autonomous measurements of 1 to 8 channels of analog data, and a schedule that can be selected to perform sampling from once every second to sampling every 19.3 hours. The sampled data is stored in the 8Kx32 FIFO register, which can be unloaded through the slave serial port interface (SPI).

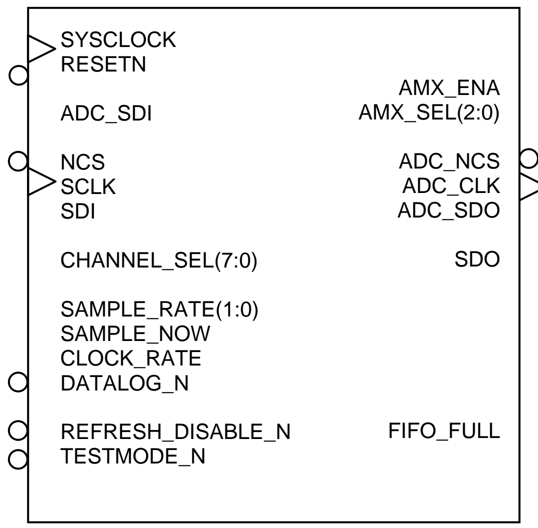


Figure 1 - MCDAC Symbol

Figure 1 shows in symbol format the primary IO. Table 1 gives a brief description of the MCDAC functional pins. Additional pins associated with the generic RPDA module are described in Table 7.

Table 1 - Functional Pin Description

Signal	Type	Function
SYSCLOCK	IN	1MHz Module Clock
RESETN	IN	Global Reset
ADC_NCS	OUT	ADC SPI Chip Select
ADC_CLK	OUT	ADC SPI Clock
ADC_SDO	OUT	ADC SPI Serial Data Out
ADC_SDI	IN	ADC SPI Data In
NCS	IN	SPI Slave Chip Select
SCLK	IN	SPI Slave Clock
SDI	IN	SPI Slave Serial Data In
SDO	OUT	SPI Slave Serial Data Out
CHANNEL_SEL(7:0)	IN	Analog Channel Mask Pins
SAMPLE_RATE(1:0)	IN	Autonomous Sample Rate
SAMPLE_NOW	IN	External Sample Command
DATALOG_N	IN	Enable/Disable FIFO
AMX_ENA	OUT	Analog MUX Enable
AMX_SEL(2:0)	OUT	Analog MUX Select Bus
FIFO_FULL	OUT	Indicates that the FIFO is full
REFRESH_DISABLE_N	IN	Enable/Disable EEPROM Refresh
CLOCK_RATE	IN	SYSCLOCK rate (1=1MHz, 0=100Khz)
TESTMODE_N	IN	Manufacturing Test Signal

2.1.1 Functional Block Diagram (Module Level)

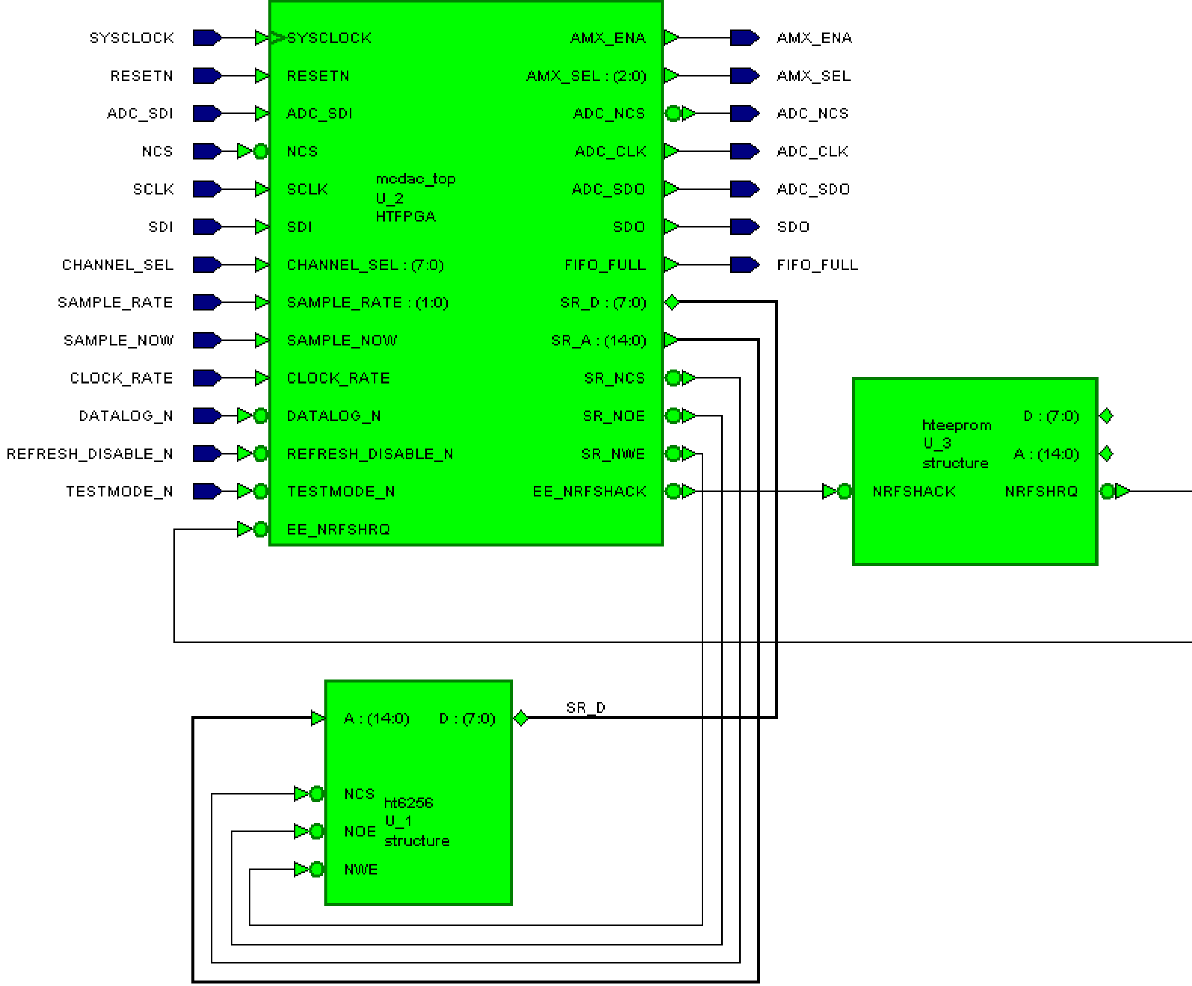


Figure 2 - MCDAC Block Diagram

Figure 2 shows the basic functional block diagram of the MCDAC implemented in the RPDA. This figure shows the representation of the SRAM which is used as the memory portion of a FIFO, and the EEPROM which is only used as the configuration boot memory for the HTFPGA. Note: RPDA connections between HTFPGA and HTEEPROM dedicated to configuration download or test and debug are not shown.

2.1.2 Functional Block Diagram (HTFPGA Configuration Level)

Figure 3 shows the MCDAC design as implemented within the HTFPGA. Primary function and operation are described in the following sections.

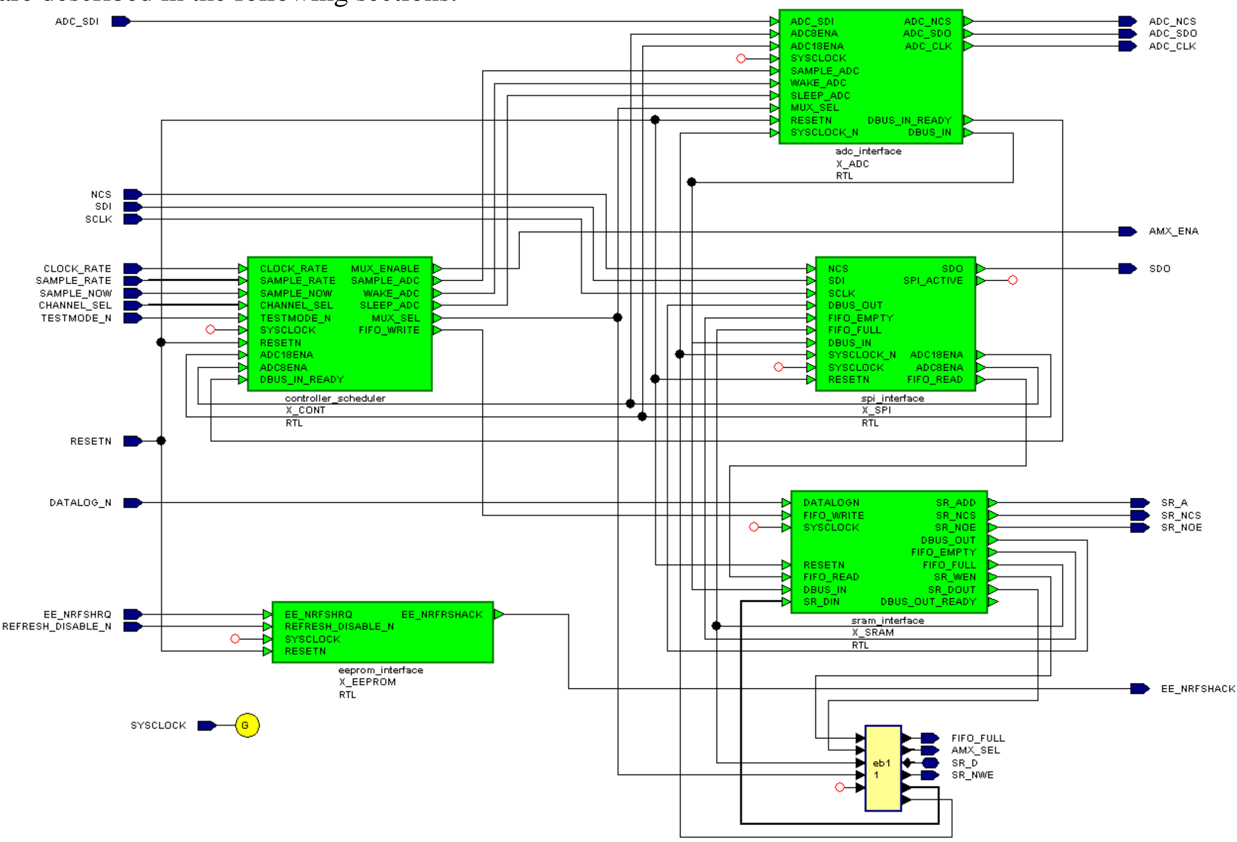


Figure 3 - MCDAC HTFPGA Configuration

2.1.3 Power-on Boot

The primary component in this module is an HTFPGA which has equivalent functionality as ATMEL's AT6010 device [4]. The HTFPGA powers up in an unprogrammed state and must go through a boot up sequence [5]. During this time, internal handshaking between the HTFPGA and the HTEEPROM loads configuration programming into the HTFPGA, programming it into the MCDAC function. In order for this to be accomplished, the user must assure that the HTFPGA mode pins are in their correct state. This is best implemented by hard wiring the M0, M1 and M2 pins to "Mode5" using VDD and VSS (see Table 3).

Table 2 - HTFPGA BOOT MODE CONTROL

Pin	"Mode 5" State	Soft Reboot
M2	1	0
M1	0	0
M0	1	0

Power-on configuration will take up to 300 milliseconds to complete, depending upon conditions. During the boot up sequence, all of the HTFPGA configurable IO will be set to a pull-up state. During the boot phase, the HTFPGA/HTEEPROM handshake will perform a self-check function to confirm that the load occurred without error. Should an error be detected, a recheck will occur. If no error in the load is detected on the second check, the ERRN flag will go high and normal functional operation will proceed. If an error is still detected the ERRN flag will remain low and the device will proceed into functional mode, however functional operation may be compromised. Figure 4 shows the general boot sequence.

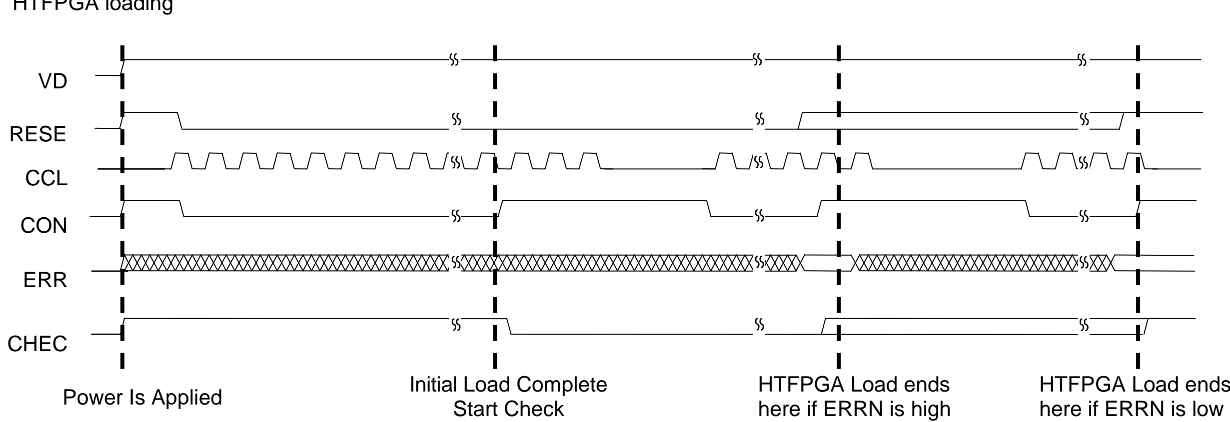


Figure 4 - Boot HTFPGA Load Sequence

Once the configuration is loaded, the internal handshaking will release RESETN and the device will respond to external stimulus and begin functional operations. The module will power up ready to collect data from both the 18-bit and 8-bit converters of the HTADC18. If the SAMPLE_RATE pins are programmed to a non-zero condition, then the unit will begin autonomous operation data collection. If the SAMPLE_RATE bus is set to all zeros, then the unit will collect data when the SAMPLE_NOW pin is toggled. Operational functions are described below.

A soft reboot of the HTFPGA can be forced by driving the M0, M1, M2 pins all to “0” and driving CONN low. This will invoke a reload of the configuration data. See the ATMEL AT6000 series application notes for further information. Most users wishing to re-initiate the module will generally do so by cycling power.

2.1.4 Slave Serial Peripheral Interface (SPI)

The Slave SPI interface allows external communication with the MCDAC, and is the means for collecting data from the module. The MCDAC will operate as a slave on an SPI bus and requires an external SPI Master to initiate data transfers using the SPI port pins.

2.1.4.1 SPI Functional Description:

The Serial Peripheral Interface Slave function provides a means for an external microcontroller operating as an SPI Master to access the results of A-to-D data logged within the MCDAC. Furthermore, the SPI

allows some features of the MCDAC to be controlled. These control functions consist primarily of the ability to enable and disable A-to-D operations to reduce power consumption. The SPI port is used to write the internal SPI Control Register and read the HTADC18 data. The status register can be read along with the data or separately. The following are the SPI port signal pins of the MCDAC:

Table 3 - SPI Port Signal Pin Definitions

Pin name	Direction	Description
SCLK	Input	Serial clock
SDI	Input	Control data
SDO	Output	ADC and Status data
NCS	Input	Low asserted chip select

2.1.4.2 SPI Protocol Defined Modes

Microcontrollers available from various vendors implement an SPI port that supports four SPI Modes of operation. The SPI Mode determines how data is exchanged using the clock and data signals of the bus. The SPI Mode is typically selected by properly programming two microcontroller programmable control bits, CPHA and CPOL, which set the SPI Mode. These modes are defined as follows:

The CPOL control bit defines the clock polarity:
0 = Active high clock pulse, low clock when idle
1 = Active low clock pulse, high clock when idle

The CPHA control bit defines the clock phase which determines clock-data relationship for data transfer.
0 = Input data is latched on leading edge of clock pulse. Output data change is triggered by trailing edge of clock pulse.
1= Input data is latched on the trailing edge of the clock pulse. Output data change is triggered by the leading edge of the clock pulse.

These are further defined as SPI mode numbers in the table below:

Table 3 - SPI MODES

Mode Number	CPOL	CPHA	Clock Pulse	Input Data Latched	Output Data Change
0	0	0	Active High	CLK rising edge	CLK falling edge
1	0	1	Active High	CLK falling edge	CLK rising edge
2	1	0	Active Low	CLK falling edge	CLK rising edge
3	1	1	Active Low	CLK rising edge	CLK falling edge

Per section 8.4, 8.5.3 and 8.5.4 of the M68HC11E Family Data Sheet Rev. 5.1, 7/2005.

The MCDAC provides a fixed implementation of the SPI Modes and mode controls and implements the SPI Mode number 3 (CPOL = 1, CPHA =1).

2.1.4.3 SPI Control/Status Register

The SPI Control Register is used to direct the operation of the MCDAC. The SPI Control/Status Register bits are set or cleared depending on the content of the SPI Control Word which is the input bit stream received over SDI, Serial Data In pin (see Table 4).

Table 4 - Control/Status Register Definitions

Bit name	Significance	Configuration Power-on state	Description
Update	Bit 7	Cleared(Low)	When HIGH, the SPI Control register gets updated
Mode(1)	Bit 6	Set (High)	When "10", gets data from FIFO. When "11", gets data most recent ADC data. When "00" or "01", only download status register
Mode(0)	Bit 5	Set (High)	
ADC18ENA	Bit 4	Set (High)	HIGH level enables the 18-bit ADC
ADC8ENA	Bit 3	Set (High)	HIGH level enables the 8-bit ADC
FIFO_FULL	Bit 2	Cleared (Low)	Indicates FIFO is full, no user input
FIFO_EMPTY	Bit 1	Set (High)	Indicates FIFO is empty, no user input
Null	Bit 0	Cleared(Low)	Reserved for future use

2.1.4.4 MCDAC SPI Output Data Formats

The primary function of the MCDAC SPI bus is to permit the retrieval of logged data. Limited control of the external ADC is also possible. To facilitate this, the MCDAC has been provided with the capability of enabling and disabling the 18-bit and 8-bit converters (noted from here on as ADC18 and ADC8). Two SPI output data formats are provided to permit data transfers with the least amount of performance overhead for the cases where: (1) the user wishes to query to FIFO status, but not perform a download (2) the user wishes to access the data that has been stored in the MCDAC. Regardless of the SPI data format selected, it is always possible to read and write the contents of the embedded SPI Control Register over the SPI interface.

The MCDAC SPI data format is set by programming the Mode(1:0) bits in the SPI Control Register as shown in the table below. An 8-bit read/write of the SPI Control Register can be made in any of these formats. The SPI data formats have been implemented so that the 8-bit status word is always read out first to provide for efficient software manipulation.

Table 5 - MCDAC SPI Output Data Format

	Mode(1:0)	Output Format
Status Register Only	"00" or "01"	8 Bits: <Status(7:0)>
Current Data	"11"	40 Bits: <Status(7:0)><SEL(2:0)><ORBit><ADC18(19:0)><ADC8(7:0)>
FIFO data	"10"	40 Bits: <Status(7:0)><SEL(2:0)><ORBit><ADC18(19:0)><ADC8(7:0)>

Key:
- Status(7:0) — Configuration register bits
- ORBit — over-range bit indicator
- SEL(2:0) — AMUX channel
- ADC18(19:0) — 18-bit ADC data
- ADC8(7:0) — 8-bit ADC Data

For the 40 bit word, the SEL and ORBit values are stored along with each ADC18 and ADC8 measurement cycle. The SEL indicates which channel was in effect when the ADC measurement occurred. A logic one in ORBit is indicates that the 18-bit ADC modulator input was over-range. See the HTADC18 data sheet [2] for further information on use and operation of this device.

2.1.4.5 SPI Status Read/Control Register Write

An 8-bit SPI Control Register Write with Status Read operation is selected when the MODE(1:0) bits are "00". The SPI Control Register write/Status Register read is initiated by asserting NCS pin LOW. The master must wait for at least four cycles of the SYSCLOCK (nominally 1MHz) before it begins clocking SCLK to begin shifting the data out of the SDO pin. The Status Register word is shifted out serially via the SDO pin, MSB first, with the SDO being updated with serial data at the falling edge of the SCLK. The falling edge of SCLK is used so that SDO data is stable and can be clocked in by the SPI Master at the next rising edge of the SCLK. The SPI Master toggles the SCLK pin LOW-to-HIGH 8 times, then SPI Master terminates the transfer by driving NCS back to HIGH level. Any SCLK clocks over the required 8 will shift zeros out the SDO pin.

When an SPI Write is used to update the SPI Control Register, the SPI Master transmits the SPI Control Word to the MCDAC over the SDI pin. The SPI Master will sequentially shift a new bit of the SPI Control Word out the SDI pin with each falling edge of SCLK beginning with the MSB bit which is shifted out first. The SPI Control Word is then transferred over the SDI and clocked into the internal MCDAC shift register using the rising edge of the SCLK to clock in the data. The SPI Control Word is latched into the SPI Configuration Register when the SPI Master drives the NCS back to HIGH but only if the Update bit of the incoming SPI Control Word is set. Any SCLK clocks over 8 will be ignored for input. If the Update bit is zero, the SPI Control Register will not be updated, though the status will still be shifted out the SDO pin. The SPI write allows the master to write in SPI Control Register concurrently with the SPI read of the previous status. The timing diagram of the MCDAC SPI Control Register write and concurrent SPI Control Register read is shown in Figure 5.

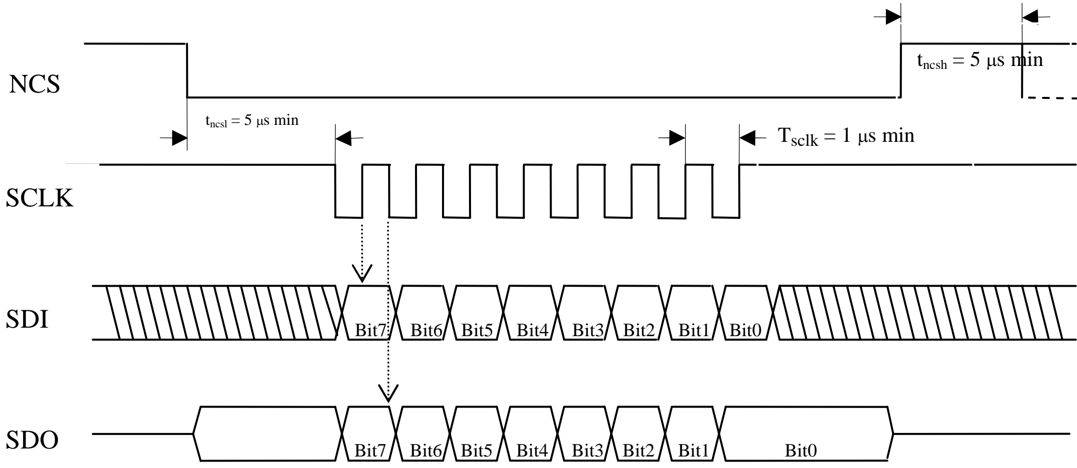


Figure 5 - SPI Control Register Write with Status Read

2.1.4.6 SPI ADC Data Reads (40-bit)

An SPI read of the ADC (FIFO or Most Recent) data can be initiated at any time. An SPI read of the ADC data is initiated by the master driving the NCS pin LOW (while still maintaining SCLK HIGH). The master must wait for at least four cycles of the SYSCLOCK (nominally 1MHz) before it begins clocking SCLK to begin shifting the data out of the SDO pin. While SPI can operate with up to the maximum specified SCLK frequency, the SPI Master must guarantee that the 8th SCLK clock cycle occurs no earlier than 12 cycles of the SYSCLOCK after the falling edge of NCS.

The MCDAC's ADC data will be shifted out the SDO pin on the falling edge of the SCLK. The output shift register driving the SDO pin is clocked out at each falling edge of the SCLK so that the corresponding data bit can be captured by the SPI Master on the next rising edge of SCLK. The 8-bit Status copy of the SPI Control Register is shifted out the SDO pin first, beginning with the MSB, and continues shifting until the LSB of the SPI Control Register data has been output. The MCDAC ADC data samples are then sent - MSB first – and output sequentially until all data bits have been shifted out the SDO pin. The SPI Master then drives SCLK HIGH followed by NCS HIGH to complete the data transfer. The SPI Master must wait for at least one cycle of the SYSCLOCK before initiating a new SPI cycle by driving NCS low.

The 8-bit SPI Control Register can also be written during the ADC Data Read transfers. To accomplish this, the SPI Master drives data to be clocked into the SPI Control Register over the SDI concurrent with the read of the ADC serial data. The SPI Master transitions the SDI data on each falling edge of the SCLK so that it will be stable for clocking into the MCDAC at the next rising edge of the SCLK. The SDI data is shifted in MSB first and loaded into an internal shift register. The SPI Control Register is updated with the shifted in Control Word when the SPI Master drives the NCS HIGH. Only the first 8 bits of SPI data are clocked into the SPI Control Register. Extraneous SDI pin input data that is associated with the additional SCLK transitions of the data 40-bit read are ignored.

A timing diagram illustrating the ADC data read and concurrent SPI Control Register write is shown in Figure 6.

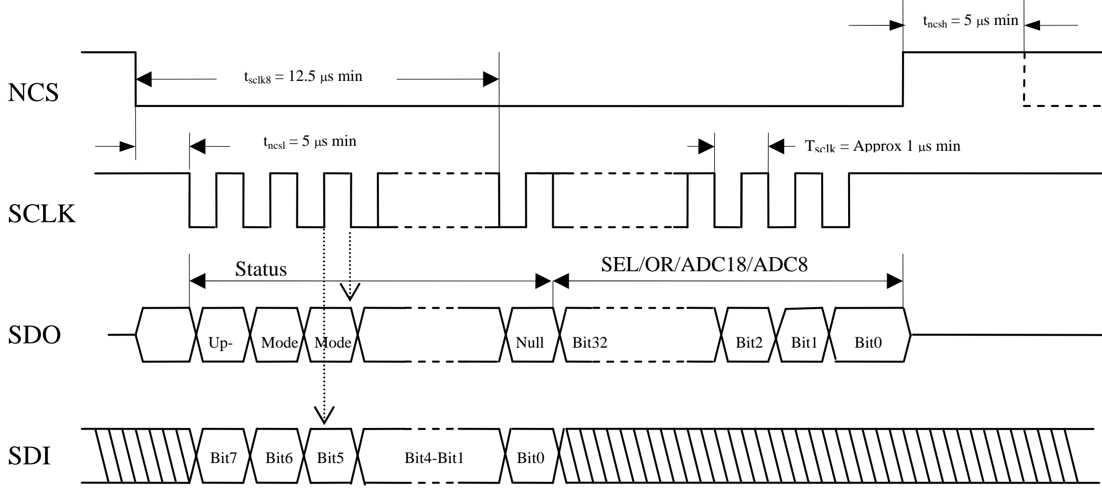


Figure 6- SPI Control Register Write with Data Read (40Bit)

2.1.5 ADC Interface

The MCDAC module has a four-port interface ADC SPI master that will connect directly to the SPI slave pins of the HTADC18. This interface will operate synchronously at SYSCLOCK rates. The ADC_CLK, ADC_NCS, ADC_SDI and ADC_SDO port should be connected to the HTADC18 SCLK, NCS, SDO and SDI pins respectively (see Figure 7).

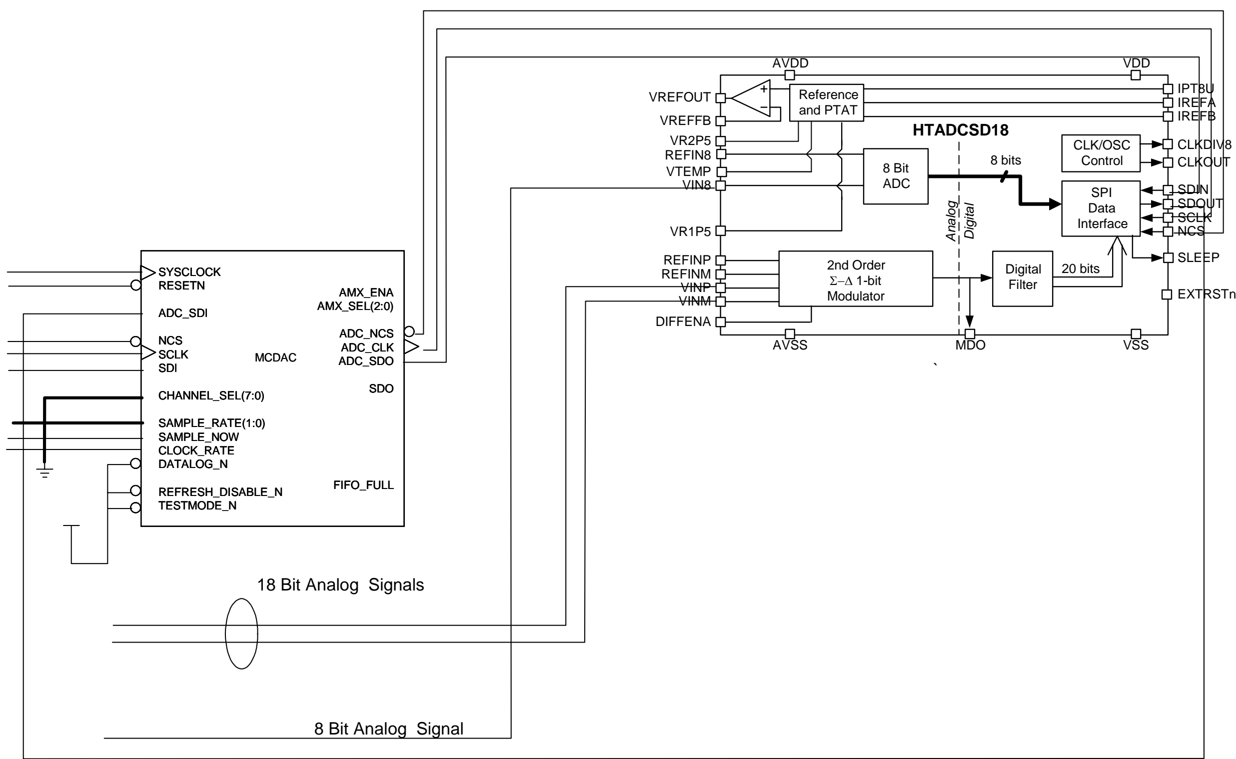


Figure 7 - MCDAC / HTADC18 Connection Diagram

2.1.6 Data Sampling Schedule

The HTADC18 uses a sigma-delta converter for the high-precision 18-bit ADC function. Per the application notes [2], the 18-bit converter requires 0.68 seconds to settle after a step function response. Because the module is intended for use in operations that switch analog inputs into the HTADC18, this step response time establishes a relatively long timing factor in the data acquisition schedule.

The MCDAC control section operates on an internally derived timer that is based on the 1MHz SYSCLOCK. The controller will step through a predefined sequence of events in which the HTADC18 is sent a wake command, data is allowed to settle, both 18-bit and 8-bit data is transferred from the HTADC18 and stored in the FIFO, and the HTADC18 is sent a sleep command. This operates on a 1-second cycle (actually SYSCLOCK_period*1E6). During the sleep period, the analog MUX channels are advanced. Once the sequence is initiated, all of the channels that are active (based on CHANNEL_SEL(7:0)) will be sampled, which can take up to 8 seconds to perform one complete datalog sequence.

Note that although the 8-bit data converter has a high bandwidth and is not limited to a minimum 0.68 second response to a step function, it will be sampled simultaneously as the 18-bit, and so will be on the same 1-second sample cycle.

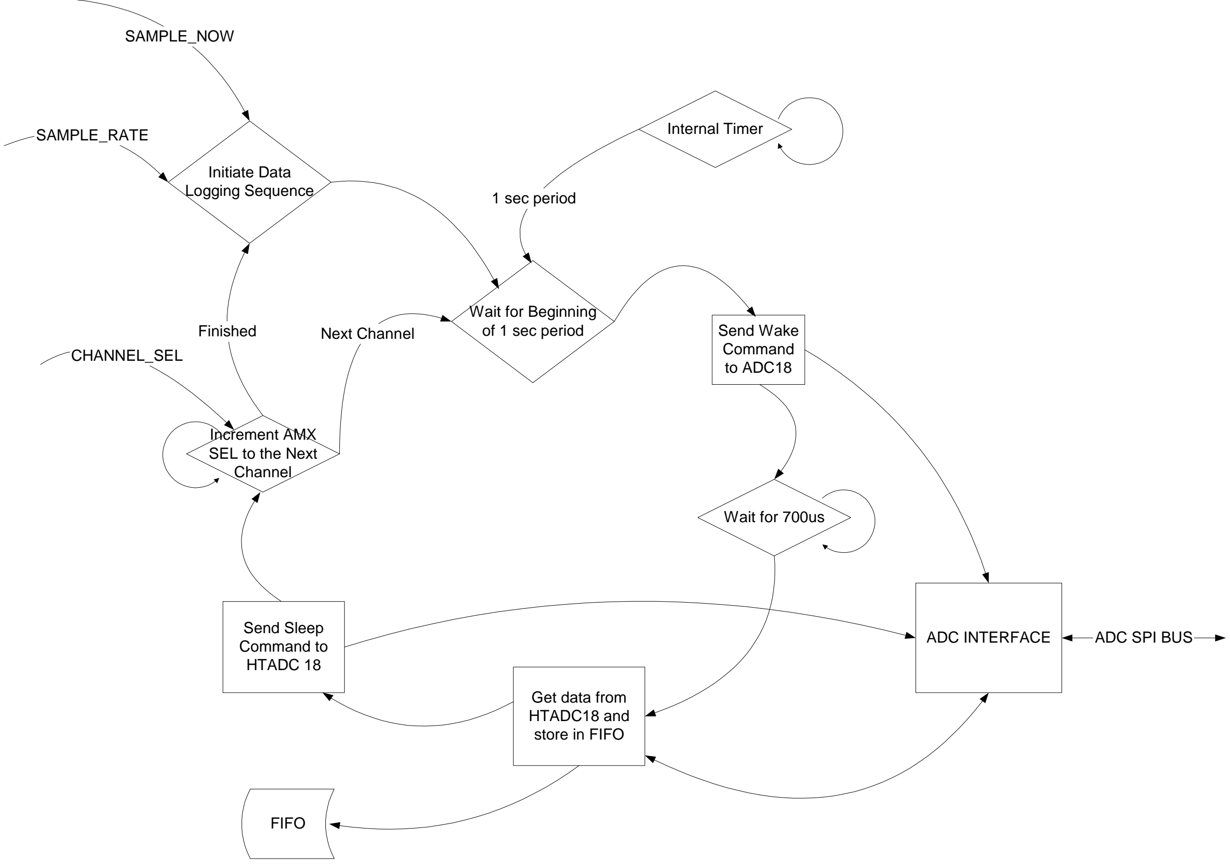


Figure 8 - State Diagram of Data Logging Function

2.1.7 Analog Data Channel Selection

The MCDAC can be programmed to direct the Analog MUX to select any combination of 1 to 8 channels. This is accomplished by setting the CHANNEL_SEL(7:0) masking pins to the appropriate states. Each bit of the CHANNEL_SEL bus corresponds to the same channel of the AMUX. Setting a particular bit to "1" will cause the MCDAC to activate that analog channel and log the data for that channel at the scheduled time. Setting the bit to "0" will cause the MCDAC to skip over that channel when performing the measurement and logging operation.

Note: if the CHANNEL_SEL(7:0) is set to "00000000", the behavior will be the same as setting it to "00000001" that is, it will not disable data measurement but will only activate and measure the first analog channel. This is intended for applications that do not need multi-channel data recording, and so can leave the AMUX out of the system.

2.1.8 Autonomous Operation

One mode of operation for the MCDAC is autonomous operation. In this mode, the internal scheduler will perform the measurement and logging sequence automatically. The period of measurement is based on the settings of the SAMPLE_RATE(1:0) bus which is used to program an internal timer. The timing of the sampling interval is derived from the following equation:

Sample_Period =
SYSCLOCK_period * 1E6 * [60 ^ [SAMPLE_RATE(1)*2 +SAMPLE_RATE(0)*1]] / (10 ^ CLOCK_RATE)

Setting CLOCK_RATE to “0” allows the use of a 100KHz SYSCLOCK while still maintaining an internal 1 second timebase. If the SAMPLE_RATE=”01”, then the sample period may be shorter than the time required to sequence through each of the channels, therefore the sample rate for each channel will be the number of channels.

If the SAMPLE_RATE(1:0) is set to ”00”, the behavior will default to Sample-On-Demand (see 2.1.9).

SAMPLE_RATE Example:
For a 1MHz SYSCLOCK, the autonomous sample period for the MCDAC is as shown in Table 6.

Table 6 - SAMPLE_RATE Selection Example for 1MHz Clock (CLOCK_RATE=1)

SAMPLE_RATE(1:0) Selection	SYSCLOCKs Between Samples (1E6 clocks)	Nominal Period (HH:MM:SS)
00	NA	Sample-on-demand
01	1	00:00:01
10	60	00:01:00
11	3600	01:00:00

2.1.9 Sample-on-Demand

The second mode of operation for the MCDAC is Sample-on-Demand. When the SAMPLE_RATE is programmed to “00”, the SAMPLE_NOW input becomes enabled. In this mode, the SAMPLE_NOW value is latched into the scheduler on rising SYSCLOCK. The scheduler maintains an internal 1 second period. At the beginning of each period, the scheduler checks for the latched SAMPLE_NOW. If the signal was detected, then the device will initiate a measure and logging sequence, sampling each of the channels as determined by the CHANNEL_SEL programming on the normal 1 sec interval. After all channels have been sampled, the module will return to a wait state, until the next time SAMPLE_NOW is toggled.

SAMPLE_NOW is latched into the module with SYSCLOCK, therefore it is necessary that the SAMPLE_NOW signal be held high a minimum of two SYSCLOCK periods in order to guarantee detection of the sample request.

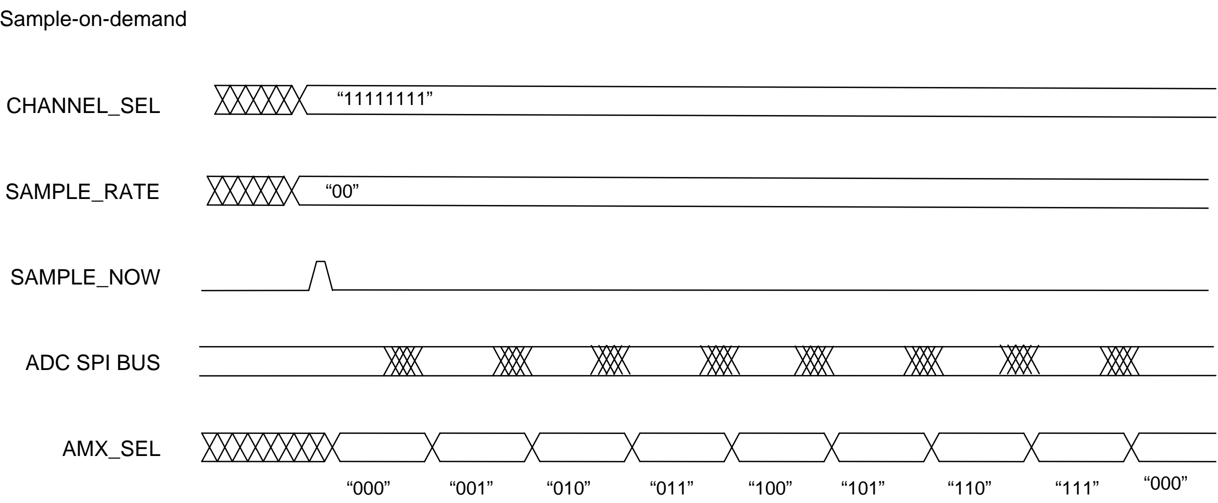


Figure 9- Data Sample Sequence

2.1.10 FIFO DATALOG_N Disable

A means of manually disabling data logging in the FIFO is provided with the DATALOG_N pin. When low, all measurements are stored in the FIFO. If the DATALOG_N is held high, then the FIFO will be disabled from writing data. The measurements will still be made, and will be available to the SPI bus for downloading (in "Recent Data" mode). This function is intended for operations in which data logging may not be desired, such as equipment insertion or extraction, or when an external set point determines that data should be logged.

2.1.11 HTEEPROM Refresh Disable

The HTEEPROM within the MCDAC implements a refresh strategy to provide reliable data retention for 5 years. Refresh circuitry will rewrite all bits in the EEPROM at power-on and then approximately once per month. An interrupt style handshake is implemented in this design so that the MCDAC is not affected by the refresh function.

The duration of the refresh process will be approximately 5 seconds. This occurs immediately upon powering up the module and after configuration of the HTFPGA has occurred. Any application that uses this component must provide power to the device for a minimum of 5 seconds to allow for the HTEEPROM function to complete. The REFRESH_DISABLE_N pin is provided for users who wish to disable the refresh function. The user must however provide some means of allowing refresh to occur regularly or risk losing the functionality of the module.

Users of this product should be aware that the HTEEPROM has a limited number of refresh cycles that can be allowed during the lifetime of the product. Applications that will undergo a large number of power cycles may exceed the write cycle limit and affect the reliability of the boot-configuration operation. These applications should take advantage of the REFRESH_DISABLE_N function wherever possible, keeping in mind the need to perform a refresh at least once every 40 days. The total allowable power+refresh cycles before impacting reliability is TBD.

3 Detail Specifications

3.1 IO Descriptions

The following table is a listing of all the signals and their purpose. Package pin mapping is shown in Table 10.

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
A12 B13 B12	M0 M1 M2	D	I	-	Mode Control For HTFPGA. User should select Mode 5 (M0=M2=VDD,M1=VSS)
A13	SYSCLOCK	D	I	-	1MHz System Clock
A14	RESETN	D	IO	-	Master Reset – Active Low
F9	CLOCK_RATE	D	I	-	Indicates to MCDAC that SYSCLOCK is either 1MHz (high) or 100KHz(low)
A6	SDI	D	I	-	Slave SPI bus controller
A5	NCS	D	I	-	Slave SPI bus controller
A8	SCLK	D	I	-	Slave SPI bus controller
A7	SDO	D	O	-	Slave SPI bus controller
A11	ADC_CLK	D	O	-	ADC Master SPI bus controller
B11	ADC_NCS	D	O	-	ADC Master SPI bus controller
A10	ADC_SDI	D	I	-	ADC Master SPI bus controller
B12	ADC_SDO	D	O	-	ADC Master SPI bus controller
B10	DATALOG_N	D	I	-	Enable Control for FIFO – Active Low
B6	FIFO_FULL	D	O	-	Indicates that the internal 8Kx32 FIFO has been filled.
G10 G9	SAMPLE_RATE1 SAMPLE_RATE0	D	I	-	Sets the autonomous sample rate. All zeros will only sample on “SAMPLE_NOW” input.
G11	SAMPLE_NOW	D	I	-	External initiation of ADC sampling. Pin is disabled when SAMPLE_RATE(1:0) is not “00”.
F8 F6 G8 G7 F5 G6	CHANNEL_SEL7 CHANNEL_SEL6 CHANNEL_SEL5 CHANNEL_SEL4 CHANNEL_SEL3 CHANNEL_SEL2	D	I	-	Controls which of the eight analog channels is recorded.

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
G5 F7	CHANNEL_SEL1 CHANNEL_SEL0				
A9	AMUX_ENA	D	O	-	Analog MUX Enable Control
B9 B8 B7	AMUX_SEL2 AMUX_SEL1 AMUX_SEL0	D	O	-	Analog MUX Select control
F10	TESTMODE_N	D	I	-	Test function. Accelerates the autonomous sample rate by 100X
F11	REFRESH_DISABLE_N	D	I	-	Disables EEPROM refresh function.
The following RPDA pins are not intended for use by the end user, and should be biased or left unconnected as indicated					
G12	UNRSTN	D	I	PU	Reboot Bypass Function. User should leave open or tie high.
C1 C2 D1 B3 B4 C3 B2 E1 F1 D2 F2 E2 G4 G3 F4	SR_A14 SR_A13 SR_A12 SR_A11 SR_A10 SR_A9 SR_A8 SR_A7 SR_A6 SR_A5 SR_A4 SR_A3 SR_A2 SR_A1 SR_A0	D	O	-	Monitor of SRAM Address. – Leave unconnected
B5 B4 C5 D3 D4 E3	SR_D7 SR_D6 SR_D5 SR_D4 SR_D3 SR_D2	D	O	-	Monitor of SRAM Data – Leave Unconnected

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
E4 F3	SR_D1 SR_D0				
A4	SR_NCS	D	O	-	Monitor of SRAM NCS - Leave unconnected.
A3	SR_NOE	D	O	-	Monitor of SRAM NOE - Leave unconnected.
B1	SR_NWE	D	O	-	Monitor of SRAM NWE - Leave unconnected.
C19 B20 C18 B19 C17 B18 E19 C16 B17 A18 C15 B16 A17 B15 D14	EE_A14 EE_A13 EE_A12 EE_A11 EE_A10 EE_A9 EE_A8 EE_A7 EE_A6 EE_A5 EE_A4 EE_A3 EE_A2 EE_A1 EE_A0	D	O	-	Monitor of EEPROM Address - Leave unconnected.
D21 C20 E20 E19 E18 E17 E16 E15	EE_D7 EE_D6 EE_D5 EE_D4 EE_D3 EE_D2 EE_D1 EE_D0	D	O	-	Monitor of EEPROM Data I/0 - Leave unconnected.
E14	EE_CSN	D	O	-	Monitor of EEPROM Chip Select - Leave unconnected.
G13	EE_OEN	D	O	-	Monitor of EEPROM Output Enable - Leave unconnected.
F14	EE_WEN	D	O	-	Monitor of EEPROM Write Enable - Leave unconnected
F13	EE_CFG_PROT	D	I	-	EEPROM - Configuration Protection – Tie to VDD
F15	EE_SELSNP	D	I	PD	EEPROM Product Interface Mode: Select Serial NOT Parallel: - Tie to VSS
G18	EE_SO	D	O	-	EEPROM Serial Data Output - Leave unconnected.

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
F16	EE_SI	D	I	PU	EEPROM Serial Data Input - Leave unconnected.
G15	EE_SCK	D	I	PU	EEPROM Serial Clock - Leave unconnected.
G16	EE_WPN	D	I	PU	EEPROM - Write Protect - Leave unconnected.
F17	EE_HOLDN	D	I	PU	EEPROM Hold/Pause of serial transmission - Leave unconnected.
G17	EE_SBP0	D	I	PU	EEPROM Serial Mode Block Protect Bit 0 - Leave unconnected.
F18	EE_SBP1	D	I	PU	EEPROM Serial Mode Block Protect Bit 1 - Leave unconnected.
G19	CCLK	D	IO	PU	HTFPGA Configuration Clock - Leave unconnected.
G14	ERRN	D	IO	PU	HTFPGA Data Validation Error - Leave unconnected.
F19	CHECKN	D	IO	PU	HTFPGA Data Validation Signal - Leave unconnected.
F20	CONN	D	IO	PU	HTFPGA Configuration Control - Leave unconnected.
A15	EE_NRFSHRQ	D	O	-	Monitor of EEPROM Data Refresh - Leave unconnected.
A16	EE_NRFSHACK	D	O	PU	Monitor of Refresh Acknowledgement - Leave unconnected.
A21	POROUTN (EEPROM PORINN)	D	IO	PU	Monitor of Power-on-Reset Activity - Leave unconnected.
E21	TM_VP	HVP	IO	-	EEPROM Positive High Voltage Supply - Leave unconnected.
C21	TM_VM	HVM	IO	-	Negative High Voltage Supply - Leave unconnected.
D17	TM_NSELALL	D	I	PU	EEPROM Select All Rows Test Mode - Leave unconnected.
D18	TM_NSELHALF	D	I	PU	EEPROM Select Half of All Rows Test Mode – Leave unconnected
D21	TM_ECC_NDISABLE	D	I	PU	EEPROM ECC Disable Test - Leave unconnected.
D15	TM_NRFSHOSC	D	I	PU	EEPROM - Refresh Oscillator Test - Leave unconnected.
D16	TM_NRFSHDIV	D	I	PU	EEPROM Refresh 30 Day Counter Test – Leave unconnected.
D19	TM_NPOE	D	I	PU	EEPROM - Parallel Outputs Enable - Leave unconnected..
D20	TMPDIODE	AG	I	-	EEPROM On-Die Temperature Diode - Leave

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
					unconnected.
A20	VSSA	AG	-	-	Analog Circuit Ground, user is to tie this to the same plane as VSS(1)
A21	VDDA	AS	-	-	Analog 5V Supply, user is to tie this to the same plane as VDD(1)
A2,G2, G20	VSS	G	-	-	Digital Circuit Ground(1)
A1,G1, G21	VDD	S	-	-	Digital 5V Supply(1)

(1) All power and ground connections should be made by low-impedance/low-inductance traces on the circuit board.

This key can be helpful in understanding some of the additional details:

Type:

D	Digital (0 = VSS, 1 = VDD) [bipad_dig]
A	Analog (varies between VSS and VDD)
HVP	High Voltage Analog, Positive (0 V to +14 V rel. to VSS)
HVM	High Voltage Analog, Minus (-14 V to 0 V rel. to VSS)
AG	Analog Circuit Ground, 0V, VSSA
AS	Analog Supply, 5 V (typ.), VDDA
G	Digital Ground, 0 V, VSS
S	Digital Supply, 5 V (typ.), VDD

Direction (Dir):

I	Input
O	Output
IO	Bidirectional, Input/Output

Pull Up and Pull Down (PU/PD):

-	None
PU	Pull Up, with type, active/resistive/current
PD	Pull Down, with type, active/resistive/current

3.2 Absolute Maximum Ratings

Table 4 – MCDAC Absolute Maximum Specifications

		Ratings(1)		
Symbol	**Parameter**	**Min**	**Max**	**Units**
VDD	Positive Supply Voltage (2)	-0.5	6.5	Volts
VPIN	Voltage on Any Pin (2, 5)	-0.5	VDD + 0.5	Volts
IOUT	Average Output Current	-20	20	mA
TSTORE	Storage Temperature	-65	250	°C
TSOLDER	Soldering Temperature (5 seconds)		355	°C
PD	Package Power Dissipation (3)		3	W
ØJC	Package Thermal Resistance (Junction to Case) 147 PGA MCM		7.0	°C/W
VPROT	Electrostatic Discharge Protection Voltage (4)	2000		V
TJ	Junction Temperature		300	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.

(2) Voltage referenced to VSS

(3) MCDAC power dissipation due to IDDS, IDDOP, and IDDSEI, plus MCDAC output driver power dissipation due to external loading must not exceed this specification

(4) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015. This is goal. ESD withstand capability has not been established for all of the components (as of Jan. 31, 2007).

(5) TM_VP and TM_VM test pins are exceptions when data is being written to the HTEEPROM. These pins are connected to the HTEEPROM internal charge-pumps and will typically be at +8.5V (VP) and -8.5V (VSS) during HTEEPROM write operations. Otherwise, during normal operation they are constrained to the voltages in the above table.

3.3 Recommended Operating Conditions

Table 5 - MCDAC Recommended Operating Conditions

			Limits		
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts
VPIN	Voltage On Any Pin (1)	-0.3		VDD+0.3	Volts
CLOAD	Capacitive Output Load			100	pF
TC	Case Operating Temperature	-55		225	°C
TJ	Maximum Junction Temperature			250	°C

(1) VP and VM test pins are exceptions, which are not for use by the user and should be left unconnected.

3.4 DC Specifications

Table 8 - DC Specifications

Symbol	PARAMETER	CONDITIONS[1]	MIN	TYP	MAX	UNITS
VDD	Digital Supply Operational Voltage		4.75	5.00	5.25	V
VDDA	Analog Supply Operational Voltage		4.75	5.00	5.25	V
IDDA	Digital Supply Operational Current	SYSCLOCK=1MHz			100	µA
IDD	Analog Supply Operational Current	SYSCLOCK=1MHz			25	mA
$IDDA_{STDBY}$	Digital Supply Standby Current	Sleep Mode, SYSCLOCK=0Hz			10	µA
IDD_{STDBY}	Analog Supply Standby Current	Sleep Mode, SYSCLOCK=0Hz			2	mA
VDD_{delta}	Supply Offset (VDDA – VDD) or (VSSA – VSS)		-0.3		0.3	V
V_{IH}	High Level Input Voltage		2.5		VDD + 0.1	V
V_{IL}	Low Level Input Voltage		VSS - 0.1		1	V
I_{IN}	Digital Input Leakage	$0 V \le V_{IN} \le VDD$	-2		2	µA
V_{OH}	High Level Output	IO = --5.73 mA	VDD – 0.5			V
V_{OL}	Low Level Output	IO = 5.25 mA			0.5	V
I_{OZ}	High-Z Output Leakage	0 V ≤ VOUT ≤ VDD	-2		2	µA
I_{OZ}	High-Z Output Leakage w/PU	0 V ≤ VOUT ≤ VDD	-600		-60	µA
C_{IN}	Input Capacitance		5	10	25	pF

Note 1 – Unless otherwise stated: 4.75<VDD<5.25, VDDA=VDD, -65C< T_{CASE} <225C, C_{LOAD} = 100pF

3.5 AC Specifications

Table 9 - AC Specifications

Symbol	PARAMETER	CONDITIONS[1]	MIN	TYP	MAX	UNITS
T_{BOOT}	Delay from Power-up to CONN Released				300	ms
F_{CLK1}	SYSCLOCK Frequency		0.1		1	MHz
F_{CLK2}	SPI SCLK Frequency		0.1		1	MHz
T_{SETUP1}	Control[2] to SYSCLOCK rising				250	ns
T_{SETUP2}	SR_D to SYSCLOCK rising				150	ns
T_{SETUP3}	ADC_SDI to SYSCLOCK rising				150	ns
T_{HOLD1}	Control[2] to SYSCLOCK rising		100			ns
T_{HOLD2}	SR_D to SYSCLOCK rising		100			ns
T_{HOLD3}	ADC_SDI to SYSCLOCK rising		100			ns
T_{DC1}	SYSCLOCK Duty Cycle		40		60	%
T_{PROP1}	SYSCLOCK falling to ADC_SDO				150	ns
T_{PROP2}	SYSCLOCK falling to ADC_NCS				150	ns
T_{PROP3}	SYSCLOCK falling to ADC_CLK				150	ns
T_{PROP4}	SYSCLOCK falling to SR_D				150	ns
T_{PROP5}	SYSCLOCK falling to SR_A				150	ns
T_{PROP6}	SYSCLOCK falling to AMX_SEL and AMX_ENA				150	ns
T_{DC2}	SPI SCLK Duty Cycle		40		60	%
T_{RISE1}	SCLK Rise Time				15	ns
T_{FALL1}	SCLK Fall Time				15	ns
T_{HIGH1}	NCS High Time		2			SYSCLOCK periods
T_{LOW2}	NCS Low Time		42			SYSCLOCK periods
T_{SETUP5}	NCS to SCLK Setup Time				150	ns
T_{HOLD5}	NCS to SCLK Hold Time		150			ns
T_{PROP7}	NCS to SDO Active Propagation Delay				150	ns
T_{SETUP6}	SDI to SCLK Setup Time				150	ns
T_{HOLD6}	SDI to SCLK Hold Time		150			ns
T_{PROP8}	SCLK to SDO Propagation Delay				300	ns
T_{RISE2}	SDO Rise Time				TBD	ns
T_{FALL2}	SDO Fall Time				TBD	ns

Table 9 - AC Specifications

Symbol	PARAMETER	CONDITIONS[1]	MIN	TYP	MAX	UNITS
T_{HIGH2}	SAMPLE_NOW High Time		2			SYSCLOCK periods

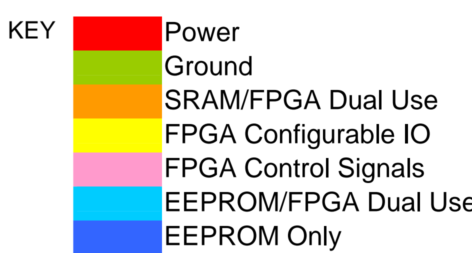
Note 1 – Unless otherwise stated: 4.75<VDD<5.25, VDDA=VDD, -65C< T_{CASE} <225C, C_{LOAD} = 100pF
Note 2 – Control Signals are CHANNEL_SEL, SAMPLE_RATE, REFRESH_DISABLE_N, CLOCK_RATE

3.6 Signal Map

Table 10 shows the mapping of MCDAC signals to package pins. Signal names are color coded to indicate their general function. Note that power, ground and functional signals are near the top and bottom edge. Test signals pins and those who are to be left unconnected by the user are located more towards the center of the package.

Table 10 - MCDAC Signal Map (Bottom View)

g01	g02	g03	g04	g05	g06	g07	g08	g09	g10	g11	g12	g13	g14	g15	g16	g17	g18	g19	g20	g21
VDD	VSS	SR_A(1)	SR_A(2)	CHANNEL_SEL(1)	CHANNEL_SEL(2)	CHANNEL_SEL(4)	CHANNEL_SEL(5)	SAMPLE_RATE(0)	SAMPLE_RATE(1)	SAMPLE_NOW	UNRSTN	EE_OEN	ERRN	EE_SCK	EE_WPN	EE_SBP0	EE_SO	CCLK	VSS	VDD
f01	f02	f03	f04	f05	f06	f07	f08	f09	f10	f11	f12	f13	f14	f15	f16	f17	f18	f19	f20	f21
SR_A(6)	SR_A(4)	SR_D(0)	SR_A(0)	CHANNEL_SEL(3)	CHANNEL_SEL(6)	CHANNEL_SEL(0)	CHANNEL_SEL(7)	CLOCK RATE	TEST MODE_N)	REFRESH_DISABLE_N	CSOUT	EE_CFG_PROT	EE_WEN	EE_SELSNP	EE_SI	EE_HOLD N	EE_SBP1	CHECKN	CONN	POROUTN
e01	e02	e03	e04	e05	e06	e07	e08	e09	e10	e11	e12	e13	e14	e15	e16	e17	e18	e19	e20	e21
SR_A(7)	SR_A(3)	SR_D(2)	SR_D(1)										EE_CSN	EE_D(0)	EE_D(1)	EE_D(2)	EE_D(3)	EE_D(4)	EE_D(5)	TM_VP
d01	d02	d03	d04	d05	d06	d07	d08	d09	d10	d11	d12	d13	d14	d15	d16	d17	d18	d19	d20	d21
SR_A(12)	SR_A(5)	SR_D(4)	SR_D(3)										EE_A(0)	TM_NRFSHOSC	TM_NRFSHDIV	TM_NSELALL	TM_NSELHLF	TM_NPOE	TMP DIODE	TM_ECC_NDISABLE
c01	c02	c03	c04	c05	c06	c07	c08	c09	c10	c11	c12	c13	c14	c15	c16	c17	c18	c19	c20	c21
SR_A(14)	SR_A(13)	SR_A(9)	SR_D(6)	SR_D(5)										EE_A(4)	EE_A(7)	EE_A(10)	EE_A(12)	EE_A(14)	EE_D(6)	TM_VM
b01	b02	b03	b04	b05	b06	b07	b08	b09	b10	b11	b12	b13	b14	b15	b16	b17	b18	b19	b20	b21
SR_NWE	SR_A(8)	SR_A(11)	SR_A(10)	SR_D(7)	FIFO_FULL	AMX_SEL(0)	AMX_SEL(1)	AMX_SEL(2)	DATALOG_N	ADC_NCS	ADC_SDO	M1	M2	EE_A(1)	EE_A(3)	EE_A(6)	EE_A(9)	EE_A(11)	EE_A(13)	EE_D(7)
a01	a02	a03	a04	a05	a06	a07	a08	a09	a10	a11	a12	a13	a14	a15	a16	a17	a18	a19	a20	a21
VDD	VSS	SR_NOE	SR_NCS	NCS	SDI	SDO	SCLK	AMX_ENA	ADC_SDI	ADC_CLK	M0	SYS CLOCK	RESETN	EE_NRFSHRQ	EE_NRFSHACK	EE_A(2)	EE_A(5)	EE_A(8)	VSSA	VDDA



3.7 Package Outline

Figure 10 shows the package outline for the MCDAC module. Note that the height dimension does not include the lid, which adds another 0.020 to the over all height.

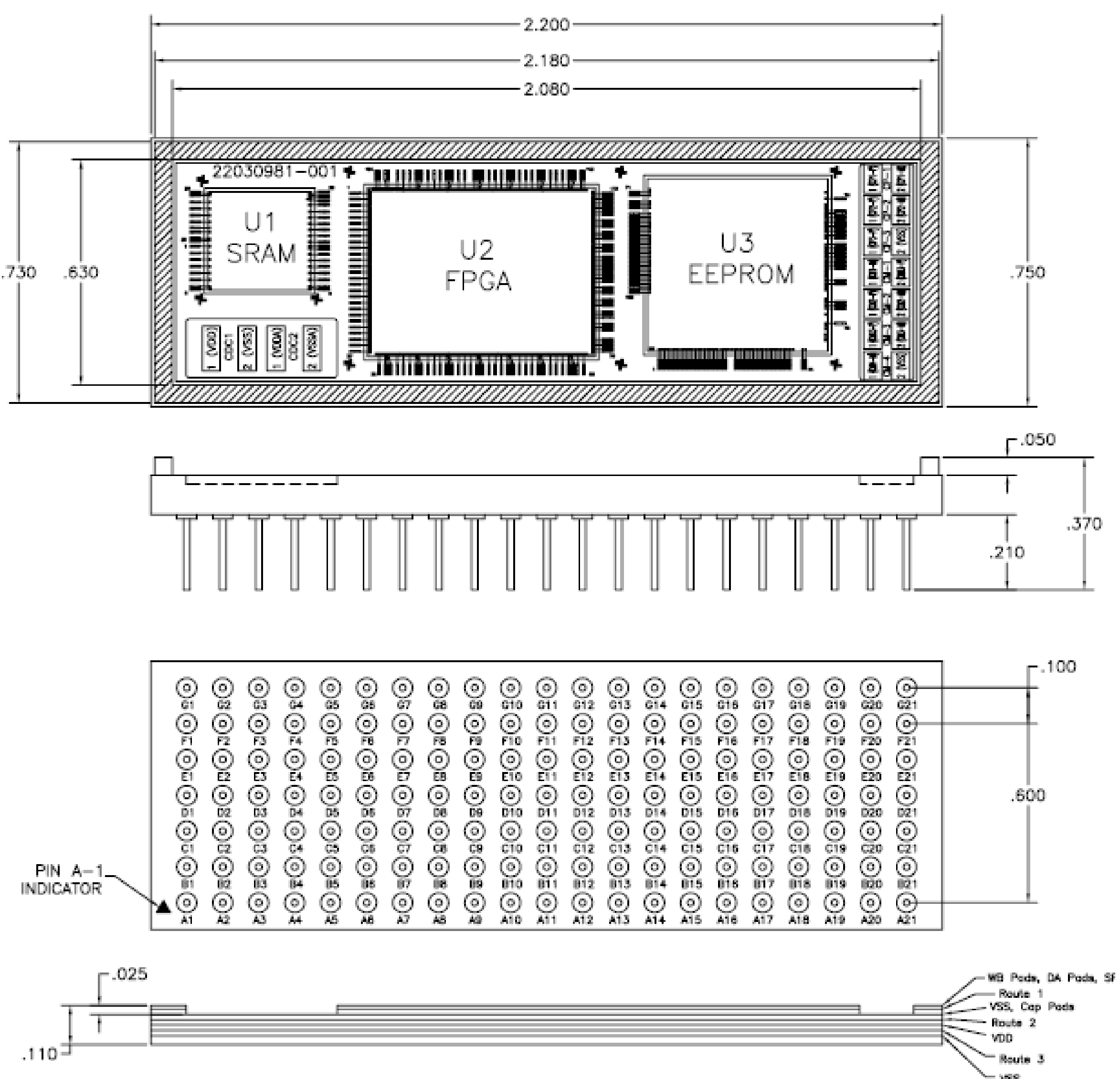


Figure 10 - MCDAC Package Outline

4 Applications

The following diagram illustrates possible modes of operation for the MCDAC.

4.1 Single Channel Operation

For applications that have limited requirements, the MCDAC can be set up in a single channel mode. Tying the CHANNEL_SEL bus to VSS will signal the unit that only one channel of data is to be recorded. If the SAMPLE_RATE is set to “01”, then the unit will log data every 1 second (at 1MHz nominal SYSCLOCK). The VIN8 pin of the HTADC18 can be tied to the VTEMP output, should one wish to monitor the on-board temperature probe of the HTADC18. See the HTADC18 datasheet for further information.

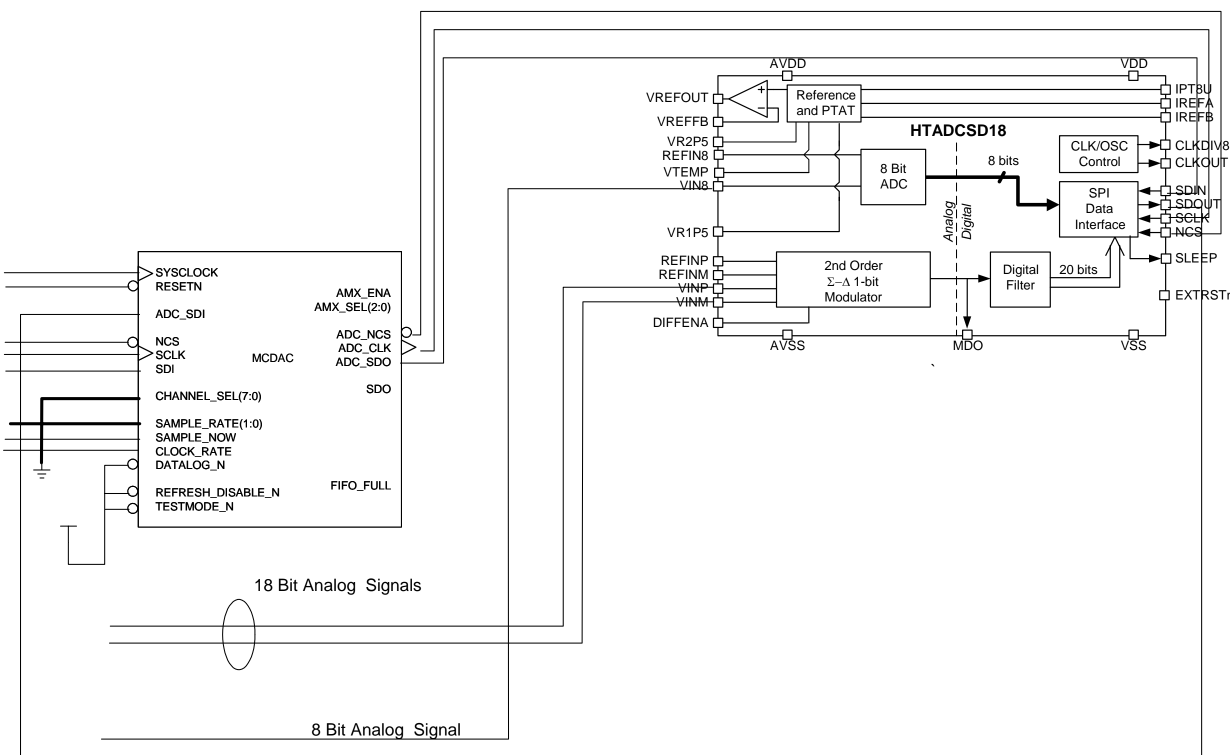


Figure 11- Single Channel Operation

4.2 Multi-Channel 18-bit Operation

For applications that require logging more channels, the MCDAC can be set up in multichannel channel mode, using an HT507 to steer differential analog inputs to the HTADC18 front end. As previously described, setting the CHANNEL_SEL and SAMPLE_RATE signals to the appropriate settings will allow multiple choices in operation.

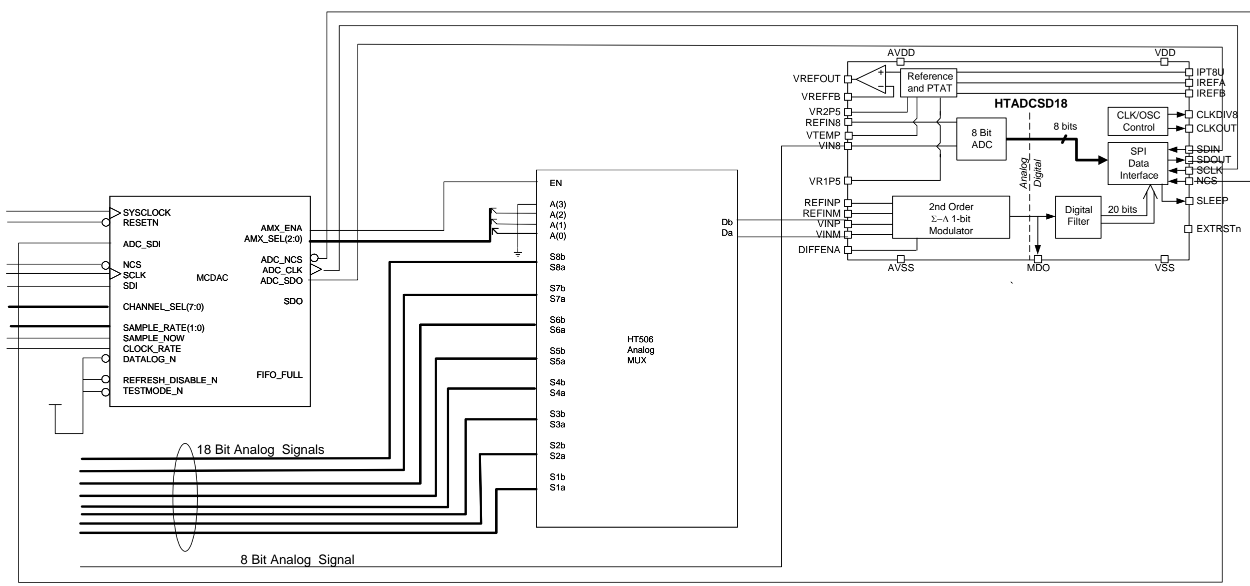


Figure 12 - Multi-channel 18-bit, Single-channel 8-bit Configuration

4.3 Multi-Channel 8-bit and 18-bit Operation

Up to two HT507 devices can be connected in parallel to the AMX pins, should an application wish to datalog multiple 8-bit data along with the 18-bit data.

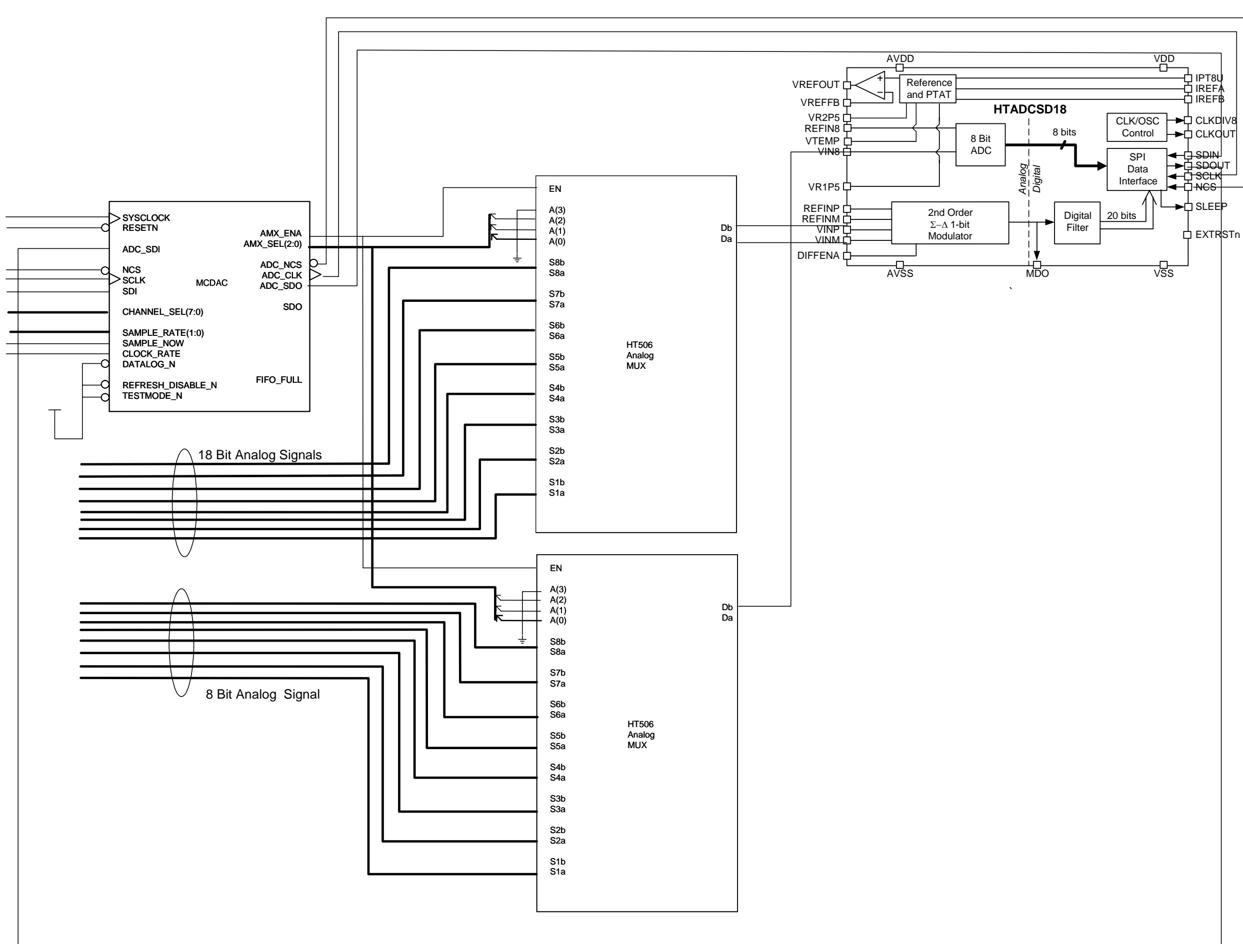


Figure 13 - Multi-channel 18-bit and 8-bit Configuration

5 References

1. Honeywell "*Reconfigurable Processor for Data Acquisition (RPDA) Data Acquisition System Objectives Specification*" Rev 1.0, dated 21 January 2007.
2. Honeywell "*HTADC18 High Temperature 18-bit Differential Input ΣΔ ADC with Built-in Clock, Voltage Reference and SPI Interface*" Datasheet dated 9-15-2006
3. Honeywell *"HT506/507 High Temperature Analog Multiplexers 16-Channel Single / 8-Channel Dual*" Datasheet – 4/98.
4. Atmel *"Coprocessor Field Programmable Gate Arrays AT6000(LV) Series"* dated 10/99
5. Atmel *"Field Programmable Gate Array Configuration Guide"* for AT6000 Series Devices, dated 9/99

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