Oil & Natural Gas Technology

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Final Report

Deep Trek Re-configurable Processor for Data Acquisition (RPDA)

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Abstract

This report summarizes technical progress achieved during the cooperative research agreement between Honeywell and U.S. Department of Energy to develop a high-temperature Re-configurable Processor for Data Acquisition (RPDA). The RPDA development has incorporated multiple high-temperature (225°C) electronic components within a compact co-fired ceramic Multi-Chip-Module (MCM) package. This assembly is suitable for use in down-hole oil and gas applications. The RPDA module is programmable to support a wide range of functionality. Specifically this project has demonstrated functional integrity of the RPDA package and internal components, as well as functional integrity of the RPDA configured to operate as a Multi-Channel Data Acquisition Controller. This report reviews the design considerations, electrical hardware design, MCM package design, considerations for manufacturing assembly, test and screening, and results from prototype assembly and characterization testing.

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Glossary and Acronyms

AC Specifications	Refers to parameters that define periodic and/or transient performance characteristics (e.g., frequency, transition times, etc.).
A-to-D or ADC	Analog-to-Digital , or Analog to Digital Converter
Atmel	A commercial supplier of integrated circuits, including FPGA's. The High-temperature FPGA design that is used in this project is a fully-licensed high-temperature version of Atmel's AT6010 product.
Behavioral Model	Refers to a structured text-based representation of a design that defines circuit functional behavior using a "Hardware Description Language" (see HDL). A behavioral model may define a design or sub-block in terms of its inputs and outputs, functionality, and timing behavior. Behavioral models describe the design at a high level of abstraction and can be used to quickly capture and simulate operation of major system building blocks.
Configuration	In this context, refers to the process or data that defines the application-specific functionality of a Field-Programmable Gate Array (FPGA).
CCLK	Configuration CLocK: This is a signal generated within the HTFPGA that is used during the configuration of the device.
CMOS	Complementary Metal Oxide Semiconductor : A term generally applied to integrated circuit processes that use two types of field-effect transistors; employing n-channel (electron) and p-channel (hole) conduction. The n-channel transistors are turned on (conduct) by applying a positive gate voltage (relative to the source terminal), while p-channel transistors are turned on by applying a negative gate voltage.
DC Specifications	Refers to parameters that can be specified in terms of static conditions, without reference to any time dimension (e.g., standby current, static drive current, input/output voltage levels, etc).
Die	An individual integrated circuit that has been cut from a silicon wafer (see "Wafers").
DOE	Department Of Energy
DWD	Diagnostics-While-Drilling
EEPROM	Electrically Erasable Programmable Read-Only Memory: A memory device that can be used to store data by electrical means (programming), that retains such data even when power is interrupted, and that can also be erased (and subsequently re-written) by electrical means.
ESD	Electro-Static Discharge
FIFO	First-In, First-Out: Refers to a type of memory structure.
Foundry	A facility providing silicon wafer processing for 3rd party designs. As an adjective describes items that are used to support 3rd party designers (e.g., "foundry toolkit").
FPGA	Field Programmable Gate Array: A digital device (Gate Array) where on-chip connections (and thereby functionality) can be defined and/or altered by the user in the field.
Gate Array	A component or design-style that makes use of predefined transistors and/or logic gate fabricated on silicon wafers where application-specific functionality is defined by the way in which the transistors or logic gates are interconnected.
Gate-level Model	Refers to a representation of a digital design that describes a circuit in terms of logic gates, flip-flops, or latches. Each of these circuit elements has a corresponding transistor-level design and physical layout that can be placed and routed within an integrated circuit.

Glossary and Acronyms (Continued)

GMS	General Manufacturing Standard: Nomenclature for Honeywell proprietary internal standards that specify recommended practices in various aspects of electronics development and manufacturing.
HDL	Hardware Description Language: Refers to one of several standard forms for describing integrated circuit behavior. Specific examples of HDL's are Verilog and VHDL.
HT2000 or HT2K	Refers to Honeywell's "High Temperature 2000" family of gate array products and/or design tools.
HTEEPROM	High Temperature EEPROM (see EEPROM)
HTFPGA	High Temperature FPGA (see FPGA)
HTSOI	High-Temperature Silicon-On-Insulator: An SOI integrated circuit manufacturing process that is optimized for extreme temperature applications (see SOI)
HTSRAM	High Temperature SRAM (see SRAM)
HW	Honeywell
IC	Integrated Circuit
GMS	General Manufacturing Standard: Nomenclature for Honeywell proprietary internal standards that specify recommended practices in various aspects of electronics development and manufacturing.
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HTSRAM	High Temperature SRAM (see SRAM)
HW	Honeywell
IC	Integrated Circuit
I/O	Input/Output
IP	Intellectual Property: Frequently used to refer to designs and/or licenses that are procured for implementation.
Masks	See "Photo-masks"
Mentor	A software company that provides design automation software for the electronics industry
MCDAC	Multi-Channel Data Acquisition Controller: The name given to the RPDA after it has been programmed (i.e., configured) to implement the functionality defined within the appendix to this report. See "RPDA" and "configuration"
MCM	Multi-Chip-Module: An integrated circuit package that house multiple chips (or "die").
MWD	Measurement-While-Drilling
NETL	National Energy Technology Laboratory – A division of the U.S. Department of Energy
Novacap	A commercial supplier of high-temperature ceramic chip capacitors

Glossary and Acronyms (Continued)

Non-volatile	In this context refers to a memory element or circuit that retains data content even if power is interrupted.
Objectives Specification	In this context refers to the document that was a Phase 1 deliverable under the cooperative research agreement between Honeywell and DOE. This document defines the objectives of the hardware and hardware configurations for the RPDA to be accomplished in this project.
PGA	Pin-Grid Array: Refers to an integrated circuit package which is constructed such that signals are presented in a 2-dimensional array of pins that project from the package body. The pins can be inserted through holes on a board-level assembly.
Photo-masks	This is generally synonymous with “masks”(Sometimes also referred to as a “reticle”). A photo-mask is a glass plate with patterns that are transferred to silicon during wafer processing by shining ultra-violet light through the photo-mask onto a silicon wafer that has been pre-treated with light-sensitive coatings. Up to 27 different photo-masks may be involved in processing a single integrated circuit.
RMP	Research Management Plan: A report mandated by the cooperative research agreement between Honeywell and DOE.
RPDA	Re-configurable Processor for Data Acquisition: The generic name for the hardware module that is developed under this research agreement.
RTL	Register Transfer Level: Refers to a means of capturing the behavior of a digital integrated circuit in terms of the data that is stored in data registers. Such a description is like a state-machine where the state changes with each clock cycle. Data is transferred between on-chip registers synchronously using one or more system clocks. An RTL description defines the registers, and how their contents are determined from one clock cycle to the next.
SRAM	Static Random Access Memory: A memory device in which data is stored at specific addresses where these addresses can be accesses in any sequence (i.e., randomly) by forcing address input bits to the desired state. A “static” memory means that a clock does not have to be running in order for the device to retain data (as opposed to a Dynamic Random Access Memory, or DRAM, which requires a clock or a minimum operating speed to function properly).
SOI	Silicon On Insulator: An integrated circuit device structure where all the transistors/devices are individually isolated by a silicon dioxide insulating layer as opposed to silicon p-n junction isolation.
SOPO	Statement Of Project Objectives: The section in DOE’s agreement with Honeywell that defines the tasks to be completed on the program.
SPI	Serial Peripheral Interface: Refers to a commonly used protocol that establishes means for serial data communication between a master and multiple slave devices.
SPICE	A generic name for a variety of commercially available circuit simulation programs. Electrical behavior is modeled at the device level (i.e., circuit elements are transistors, resistors, capacitors, etc.)

Glossary and Acronyms (Continued)

SRAM	Static Random Access Memory. Refers to a data memory circuit where the data can be randomly accessed by means of the data "address" inputs. "Static" refers to the fact that the memory retains data as long as power is applied without any requirement for periodic "refreshing" (i.e., re-writing) the data.
Synthesis	In this context, synthesis refers to the process of creating a Gate-level Model of a design that is functionally equivalent to a Behavioral or Register-Transfer-Level (RTL) representation of that design.
TBD	To Be Determined
TSA	Technology Status Assessment: A report mandated by the cooperative research agreement between Honeywell and DOE.
Volatile	In this context, refers to memory or a circuit that can store data as long as power is applied, but where that data is lost if power is interrupted.
Wafers	Specially prepared sections of single-crystal silicon that are processed to produce integrated circuits. Wafers on this program have a 6-inch diameter and are approximately 675 microns thick. Many individual integrated circuits are produced on a wafer and these are cut apart at the completion of wafer processing.
WBS	Work Breakdown Structure

1.0 Executive Summary

High-reliability, high-temperature packaging is an essential element of down-hole electronic systems. Co-fired ceramic Multi-Chip Modules (MCM's) can meet this need with stable performance at temperatures greater than 225°C.

An MCM can be likened to an electronics board implemented in a single solid piece of ceramic material. Layers of ceramic material (Alumina, Al_2O_3) are alternated with patterned layers of interconnect metallization (such as Tungsten) that are built into a multi-layered structure and then fired to result in a single, hermetic ceramic package. Multiple die can be housed in such a package using high-temperature adhesives and wire-bonded to internal package interconnect traces. External pins are brazed onto the ceramic body where external metallization is plated with gold for long-term high-temperature applications. Lids made of Kovar (Ni-Fe-Co) that are well matched to the thermal expansion properties of the ceramic are welded to Kovar seal rings built into the ceramic. This technology results in high density, hermetically sealed package with short internal wire lengths that is extremely tolerant of shock and vibration and capable of withstanding extreme temperature cycles.

Under this project, Honeywell has developed an MCM to house several High-Temperature Silicon-on-Insulator (HTSOI) integrated circuits and nine ceramic chip capacitors in a package with 147 pins. The physical design of the package is tailored to down-hole applications in terms of physical dimensions, wide operating temperature range, and ability to withstand high shock and vibration environments. The integrated circuits included in the package are chosen to provide capability equivalent to a simple, flexible micro-controller with built-in non-volatile instruction memory and data memory in a single package. This capability has been demonstrated by configuring it as a Multi-Channel Data Acquisition Controller (MCDAC) that can be used with other HTSOI components developed for down-hole data acquisition applications. This intended application leads to the title of this project, *Reconfigurable Processor for Data Acquisition,* or RPDA.

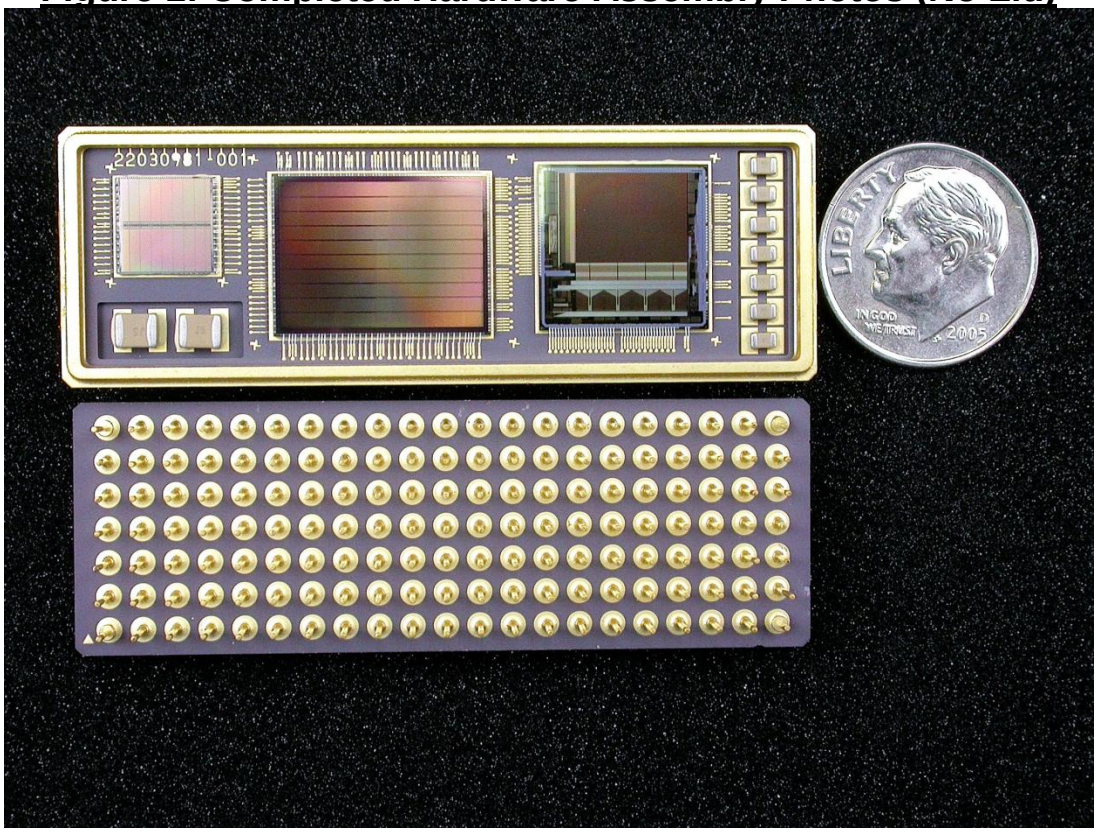
The integrated circuits were fabricated using silicon on insulator process technology specifically developed for extreme temperature applications. This high-temperature wafer process was upgraded to production status under a previously completed Deep Trek cooperative research agreement (DE-FC26-03NT41834). That same program included development and prototyping for two of three integrated circuits used in this project. These are a 32K word by 8-bit non-volatile memory (HTEEPROM), and a 30,000 gate high-temperature field-programmable gate

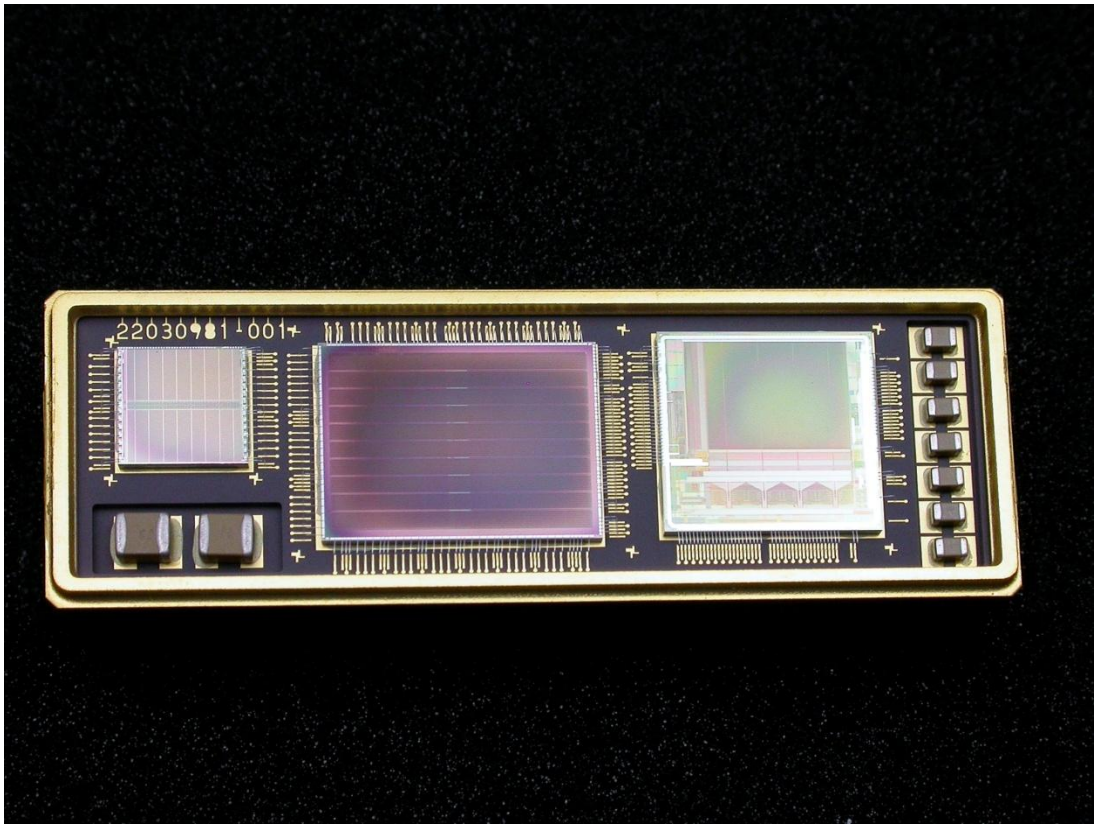
array (HTFPGA). The HTFPGA is the key programmable element within the RPDA. It is functionally equivalent to a commercial field-programmable gate array (FPGA), the Atmel AT6010. However, unlike the AT6010 it is capable for reliable operation at up to 250°C. The third integrated circuit is 32K word by 8-bit static RAM (HT6256 SRAM), which is fabricated and sold by Honeywell commercially.

As this project unfolded, it was learned that the HTEEPROM, designed and fabricated under the previous DeepTrek project (DE-FC26-03NT41834) was non-functional (due to design issues). Because the HTEEPROM was vital to meeting the objectives of this project, a revised project plan was proposed and accepted by the DoE. This revision allowed for the necessary re-design, fabrication, and testing so that functional HTEEPROM die could be provided for the demonstration objectives of this project. Life-testing of assembled RPDA units was deleted from the program scope in order to make this possible within the available project budget.

The project is now complete, and has succeeded in meeting almost all of the objectives that it was intended to meet. The MCM package has been designed and fabricated. The HTEEPROM has been successfully re-designed, fabricated and tested. RPDA prototypes have been assembled using high-temperature SOI integrated circuits and capacitors (See Figure 1). These have been configured using configuration code developed specifically for this project, and tested to verify the integrity of the package design and construction, the internal components, and the configured functionality. The result is prototype demonstration of a re-programmable device with an operating temperature range up to 250°C that can be used to implement a wide range of digital functionality in rugged package suitable for deep down-hole oil and gas well-logging, MWD, and permanent installation applications.

Figure 1: Completed Hardware Assembly Photos (No Lid)





2.0 References

1. RMP-NT42947: *Research Management Plan for Deep Trek Re-configurable Processor for Data Acquisition*, December 4, 2006.
2. TSA-NT42947: *Technology Status Assessment for Deep Trek Re-configurable Processor for Data Acquisition*, February 26, 2007
3. *Data Acquisition System Objectives Specification*, DOE Award DE-FC26-06NT42947, Deep Trek Re-configurable Processor for Data Acquisition (RPDA), January 31, 2007
4. Topical Report - Phase 1 (Final Report of Phase 1) Deep Trek Re-configurable Processor for Data Acquisition (RPDA), October 12, 2007.
5. Atmel "Coprocessor Field Programmable Gate Arrays / AT6000(LV) Series", Rev. 0264F–dated 10/99
6. Atmel "Field Programmable Gate Array Configuration Guide" for AT6000 Series Devices, dated 9/99
7. Honeywell *"HT2000 Data Book"* revision 11-11-2005.
8. Honeywell "*HIGH TEMPERATURE 32K x 8 STATIC RAM (HT6256)*" datasheet, rev. B, dated 4/98
9. *RPDA Characterization Report,* DOE Award DE-FC26-06NT42947, Deep Trek Re-configurable Processor for Data Acquisition (RPDA), September 18, 2009.

3.0 Technical Approach

The objective of this project is the specification, design, prototype fabrication and testing of a High-temperature, re-programmable electronics module that can be configured to provide a wide range of digital functions in a package suitable for down-hole oil and gas exploration tools and production well monitoring. This is accomplished by the development of a High-temperature ceramic multi-chip module (MCM) package to house previously developed High-temperature integrated-circuits consisting of:

- an SRAM (Static Random-Access Memory) commercial die developed by Honeywell [reference 7]
- an EEPROM (Electrically-Erasable Programmable Read-Only Memory) prototyped under a previous Deep Trek project led by Honeywell (DOE Award No.: DE-FC26-03NT41834)
- an FPGA (Field-Programmable Gate Array), also prototyped under the previous Deep Trek project.

Interconnection between these components and to/from the external device pins is provided by multi-layer routing that is embedded within the ceramic package body. Pins are brazed to the external connection points on the surface of the ceramic body. The IC components are attached by high-temperature epoxy to metalized die-mounting pads in a cavity formed within the ceramic package. A combination of conductive and non-conductive epoxy is also used to attach required ceramic chip capacitors to metalized terminals within the package cavity. Aluminum wire-bonding techniques are used to provide connections between wire-bond pads on the integrated circuits and metalized wire-bond pads on the surface of the package cavity. A metal lid is welded to the top of the package in order to hermetically seal the components within.

The re-programmable digital functionality is realized by the High-Temperature FPGA (HTFPGA). The configuration of this device is accomplished by loading configuration from a non-volatile memory device, in this case the High-temperature EEPROM (HTEEPROM). The HTEEPROM is specifically developed to provide this capability. Additional capacity within the HTEEPROM provides additional non-volatile data storage. Memory capability to support processing functions is provided by means of the High-temperature SRAM.

Beyond the design and verification of the MCM package, this project further demonstrates the re-configurable processing capability of the RPDA module by developing a configuration file for the FPGA, and demonstrating the ability to embed the configuration file within the EEPROM in such a way that the RPDA module autonomously configures itself on power up. The project further involves developing test hardware and software for the RPDA, and its use for testing prototype RPDA modules.

The overall technical approach for this project has been described in more detail within the Research Management Plan [reference 1]. The Research Management Plan (RMP) organized the work of this project into 15 tasks, split into two phases. As the project continued, the contract Statement Of Project Objectives (SOPO) was amended and re-stated to add tasks 16 and 17, and remove Task 14. The resulting top-level Work Breakdown Structure is shown below.

Phase 1 Activity (Feasibility Concept Definition & Proof of Concept)

Task 1: Research Management Plan
Task 2: Technology Status Assessment
Task 3: Data Acquisition System Objectives Specification
Task 4: Digital Sub-system Specification and Design
Task 5: Test Specification
Task 6: MCM Package Design and Layout
Task 7: Phase 1 Program Support
Task 8: Prepare Phase 1 Final Report

Phase 2 Activity (Prototype Development and Testing)

Task 9: MCM Package Procurement
Task 10: RPDA Test Hardware and Software Development
Task 11: Components to Support Assembly of RPDA Prototypes
Task 12: RPDA Assembly
Task 13: RPDA Characterization Testing
Task 14: RPDA Life Test and Report (REMOVED)
Task 15: Phase 2 Program Support
Task 16: HTEEPROM Design Verification
Task 17: HTEEPROM 2nd Pass Development and Fabrication

The Phase 2 task modifications (executed by SOPO amendment) were made necessary due to issues with the HTEEPROM die that were produced under the previous Deep Trek project (DE-FC26-03NT41834). The original plan assumed that residual die from that project would be used for this project. However, these HTEEPROM die were not functionally verified under that project. Therefore Task 16 wafer added in order to verify suitability of those die for the purposes of this project. The outcome of that task was a finding that those HTEEPROM die were non-functional. Therefore a design revision of the HTEEPROM component was required. This has been accomplished by the addition of Task 17.

These additional tasks were added to the project without increase to the project cost. This was accomplished by adjustment in scope of other Phase 2 tasks as follows:

- Task 11 was modified in scope. As originally envisioned, HTFPGA wafers were to be fabricated to produce the HTFPGA die needed for this project. Instead, residual die from the previous Deep Trek project were obtained from DoE/NETL and Honeywell and used for the prototype assembly.
- Task 14 was removed from the program.
- The number of units assembled in Task 12 and the scope of testing performed in Task 13 was adjusted in order to conform to the available budget.

4.0 Results

Phase 1 activity was completed essentially as it had been laid out in the Research Management Plan [Reference 1]. Phase 1 results have been previously reported in the context of the Phase 1 Final Report [Reference 4]. In this document, results of Phase 1 activity are reprised in abbreviated detail relative to that report.

4.1 Phase 1 Results

4.1.1 Task 1: Research Management Plan

The Research Management Plan (RMP) was a scheduled deliverable of this project. It was completed and published in December 2006 [Reference 1]. It addressed the project execution plan, including project staffing and management, technical objectives, WBS, budget, milestones, schedule, and deliverables.

4.1.2 Task 2: Technology Status Assessment

The Technology Status Assessment (TSA) was another scheduled deliverable of this project. It was completed and published in February 2007 [Reference 2]. It addressed the current state of technology relative to the project objectives, development strategies to be employed, and potential future impact upon successful completion of the project.

4.1.3 Task 3: Data Acquisition System Objectives Specification

The Objectives Specification was another scheduled deliverable of this project. It was completed and published in January 2007 [Reference 3]. It was developed to serve as a preliminary specification to guide the electrical and package design activity within the project. It also defined objectives for a target configuration of the RPDA module that would demonstrate the Data Acquisition mission objectives for this project.

4.1.4 Task 4: Digital Sub-system Specification and Design

This task was completed during Phase 1, with the objective of specifying the electrical operating environment, electrical connectivity of the MCM, and (via simulation and/or other analysis) to verify that the electrical design was consistent with the objectives, as captured within the Objectives Specification [Reference 3]. In order to make these objectives meaningful, a functional specification was developed for a hypothetical target application, namely a Multi-Channel Data Acquisition Controller (MCDAC).

The electrical design incorporates three High Temperature Silicon-on-Insulator (HTSOI) integrated circuits and nine ceramic chip capacitors in a ceramic package with 147 pins. The internal components are:

- HTFPGA – Honeywell Part Number 22027498
- HT EEPROM – Honeywell Part Number 2203092
- HT6526 – Honeywell Part Number 22019256
- Two 0.1uf power supply decoupling capacitors – Novacap 1210H104M250PH or equivalent
- Seven 10nf charge pump capacitors – Novacap 0805H103M500PH or equivalent

The block diagram for the RPDA showing these components and their connection is shown in Figure 2. There are up 112 programmable I/O. This includes up to 55 fully configurable I/O plus 57 I/O with direct access to SRAM/EEPROM bus that can also be configured by the user. It is projected that that the RPDA will function reliably at system clock rates up to 10MHz from a single 5V supply, utilizing CMOS I/O levels [reference 7].

Configuration can be accomplished in multiple modes (using configuration modes 1, 2, and 5 as defined within Reference 6).

Many of the electrical design considerations were dictated by the electrical design characteristics of the previously developed IC components. These included Operating conditions (Table 1), and Absolute Maximum Rating (Table 2). The electrical connectivity between components and the MCM pin-out requirements were also defined. Except for a few minor changes, these were carried forward without change into the final design. The final connectivity is in accordance with Table 3.

This task also incorporated a significant level of simulation and configuration tool development in order to insure the inter-operability of the components, and the capability for configuring the hardware to a specific functional objective. This work included:

Configuration Tool Verification and Validation: The High-temperature Field Programmable Gate Array (HTFPGA) is functionally equivalent to the Atmel AT6010 product [Reference 5]. In order to configure the FPGA for use, a configuration file is down-loaded into memory locations on the chip [Reference 6]. This is done in accordance with software provided by Atmel. This software and associated data specific to the RPDA were installed and verified.

HTFPGA Design Database Validation: The un-configured HTFPGA consists of a structured set of Configurable Logic Blocks (CLBs') that have within them logic gates, multiplexers, functional data storage elements (Flip-flops and/or latches), and configuration memory cells (configuration RAM). The functionality within a CLB, as well as CLB inputs and outputs are modified according to the data that is stored in the configuration RAM cells. The HTFPGA also contains means for using dedicated interfaces to down-load configuration file data from an external source and route it to CLB configuration memory throughout the chip as required to implement the required functionality.

A gate-level structural netlist (corresponding) to the "un-configured" structure of the HTFPGA) was developed in Verilog simulation format and verified by simulation, including simulation the configuration process as well as subsequent simulation of configured behavior. Normally post-configured behavior will be simulated using at higher levels of design abstraction (such as behavioral). Simulation at the behavioral level is much more efficient in terms of simulation time and resources relative to a strictly gate-level or structural simulation.

As a first step in validating the HTFPGA design netlist gate-level simulation was completed using the same test patterns that are applied in wafer-level testing of the HTFPGA die. Expected behavior of the design was observed by simulation of min/max timing parameters annotated to the netlist via Standard Delay Format (SDF) timing files. A primary objective of this level of detailed simulation is to verify that the HTFPGA can be configured in multiple modes and perform as intended after configuration. These test cases included boot-up and reset simulation in configuration mode 5 (autonomous configuration) and mode 1 (address count-up, external configuration clock) followed by functional testing of configured behavior. In addition boot-up and reset simulations were completed for mode 2 operation (address count-down, external configuration clock).

Simulation test benches were also generated to verify the self-checking functions associated with HTFPGA configuration.

RPDA Top-level Design Simulation: The inter-connection of all of the internal components within the MCM was fully defined in the form of top-level VHDL netlists. The top-level design was then simulated using VHDL simulation tools. In particular, the gate-level structural viewpoint of the HTFPGA has been simulated along with behavioral models of the HTEEPROM and HTSRAM models. Features were added to the HTEEPROM model to emulate the configuration down-load interface. One of the primary objectives of these simulations was to verify the functionality of the HTEEPROM / HTFPGA power-on autonomous configuration download. It was in the course of this simulation that failure to download configuration data from HTEEPROM to HTFPGA was revealed (as discussed in the summary section above), leading to the initiation of project re-planning activity to incorporate additional HTEEPROM assessment and eventually re-design..

RPDA Firmware (MCDAC Target Configuration) Development: Behavioral models of the targeted functionality (Appendix 1) were developed and simulated. Then, using Atmel configuration tools, a gate-level netlist with equivalent behavior has been developed. The gate level netlist is further processed to "place-and-route" the gates within the configurable logic blocks by means of a configuration file generated by Atmel tools in conjunction with timing files specific to Honeywell's HTFPGA.

Several tools have been used in the process of progressing from pre-configured simulation and analysis of the RPDA, (focusing especially on the HTFPGA) to generation of a configuration file to implement the MCDAC configuration:

Schematic Capture and Simulation Tools:

- Mentor DA en 2002: HTFPGA Schematic capture
- QSimPro 2004SP5: HTFPGA QuickPart (gate/transistor level) simulation
- Modelsim 5.8d: HTFPGA QuickPart (gate/transistor level) simulation
- Modelsim 6.1e – HTFPGA and RPDA Hardware Description Language (HDL) simulation

Synthesis and Routing Tools:

- Mentor Leonardo Spectrum 2006b.12: Gate-level structural synthesis
- Atmel Figaro IDS7.6.7: Place and route and timing analysis; used with a software patch specific to the HTFPGA (AT6010HLV-010QM)

4.1.5 Task 5: Test Specification

The objective of this task within Phase 1 was to assess the design and testability of the RPDA, (both before and after configuration) in sufficient detail to ensure that the test requirements of the project could be met, and also to support eventual production-level testing.

Test assessment for the RPDA takes into account the following:

- All of the signal routes connecting internal components are brought out to RPDA package pins (except for HTEEPROM charge-pump capacitors)
- It is assumed that sufficient fault coverage of individual components will be provided by wafer-level testing prior to assembly within the RPDA. Fault coverage for individual components is expected at 99% or more.
- All of the internal devices can have their outputs tri-stated (i.e., put into a high-impedance state) so that each internal component can be individually tested in situ.
- HTEEPROM test pins are brought out to monitor Error Correction features, test the memory refresh timer, and enable global memory and block writing.
- Configuration data can be loaded directly into the HTFPGA via external interfaces for manufacturing test purposes.
- Configuration data can also be loaded into the HTEEPROM either through the HTEEPROM parallel interface or the HTEEPROM serial interface.
- All of the HTFPGA I/O DC parametric testing is envisioned as a functional state machine that sequences through a standard set of tests. For example:
    - Configure all I/O as inputs except one that is configured as an output, where all the inputs are connected to the output via an AND tree in order to test input logic levels (VIH/L)
    - Configure all I/O tri-stated outputs. Measure stand-by current and High-impedance output currents (IDDSB,IOZ)
    - Configure I/O with one input, remainder connected via a serial scan register. Measure output logic levels (VOH/VOL)
- Configure HTFPGA as a direct “pass through” port to the SRAM. Verify interconnect to/from SRAM by read/write via the HTFPGA port.
- Configure HTFPGA as a direct “pass through” port to the HTEEPROM. Verify interconnect to/from HTEEPROM by read/write via the HTFPGA port.
- A temperature-dependent diode on the HTEEPROM is bonded out to enable characterization of internal temperature rise.

It was determined as a result of these considerations and other assessment that no special test circuits are necessary. The RPDA pin-out and functional architecture along with test features built into the individual components result in a highly controllable and observable structure. However, the initial finding was slightly modified by the observation (confirmed by Honeywell the other MCM products) that the Automated Test Equipment (ATE) in their current form would not be able to exercise product test at (or above) the required operating temperature range of the RPDA. This led to the approach (implemented during Phase 2) of incorporating a heater within the RPDA package itself.

4.1.6 Task 6: MCM Package Design and Layout

A detailed MCM package design was completed in during Phase 1 and reviewed at the Preliminary Design Review (PDR). This review included detailed information regarding component dimensions, wire-bond pad placement, electrical connectivity, pad-assignments, layer-definitions and thicknesses, as well as materials, test interfaces, and assembly-process requirements. .

The MCM materials and assembly technology are based on prior successful experience with high-temperature. Proven materials and processes include:

Package Type:	High Temperature Co-fired Ceramic MCM
Package Body:	90% Al_2O_3 Multi-layer
Internal Metallization:	Tungsten
Pins, Seal Ring, Lid:	Kovar (Fe-Ni-Co)
External Metal (Plating)	Gold (80µin.) over Ni
Die Attach:	Conductive adhesive
Capacitor Attach:	Conductive and Non-conductive adhesives
Wirebond:	Ultrasonic Al wedge Bond
Hermetic Seal:	Welded Kovar Lid

The MCM materials and sealing process are capable for temperatures in excess of 300°C. Die and capacitor attach adhesives have been used in similar package applications with an adhesive curing temperature of 300°C and burn-in and life testing at 250°C. Residual Gas Analysis (RGA) of previous package designs demonstrates that adhesives pass requirements of less than 5000 PPM after 1000 hour life test. Thermal conductivity of the package materials should result in internal self-heating of less than 5°C/W (junction to case).

There are no significant internal sensitivities of the RPDA design from a signal cross-talk or signal routing consideration. The MCM interconnect is routed using three power/ground planes and three signal routing layers (not including the layer later added for routing the heater element in the package).

Digital VDD and VSS for all three internal components are brought in through 3 pairs of pins and routed using the power/ground planes. There is provision for two 0.1uF supply de-coupling capacitors within the package.

Analog VDDA and VSSA are routed separately to the HTEEPROM to power charge-pumps used to create high voltage supplies used for writing to the HTEEPROM. These are very low current draw (10uA) and do not require special routing.

MCM signals are routed within a given plane at 5 mil spacing or separated from other signals by power/ground planes. Long routes and cross-overs are minimized by placement of the HTFPGA between the HTEEPROM and HT6256 SRAM, and by the intentional design of the HTEEPROM placing signals that are used with the HTFPGA on the side of the HTEEPROM die that is adjacent to the HTFPGA.

Maximum coupling between digital signals at 3.5pF/cm of routing trace would be 10pF which is not considered to be an issue. Power/Ground routing within the MCM has been accomplished by dedicated power/ground planes, so that there will be no significant internal power/ground voltage drops. At the frequencies and power-dissipation levels anticipated for this design, it is expected that I/O characteristics will be primarily determined by the internal components rather than by the package design.

Package pins are arranged on 100mil centers. Normal board routing procedures will be applicable without issues.

The MCM design assumed that the high-temperature conductive adhesive would be employed for die attach. However, gold-eutectic die bonding is also an option. Electrically conductive die bonding will be employed to ensure that the die backside is at a known electrical potential. All die bond surfaces within the package will be electrically connected to VSS (ground).

Assembly materials and processes have generally been proven on prior designs, and so there are no new assembly processes to be developed. An assembly process flow was compiled citing pre-existing documented operating procedures.

After the PDR only minor changes were identified for the package design. These included the plan to incorporate a heater into the MCM package design, which was implemented during Phase 2 activity

4.1.7 Task 7: Phase 1 Program Support

On-going program management support was provided in Phase 1 for active tracking, monitoring, technical coordination and progress reporting. The Phase 2 execution plan has was updated.

Phase 1 Program Support also included attendance/presentation at the Kick-off Review (29-November, 2006) and the Phase 1 Exit Review (12-September-2007), both at DoE/NETL in Morgantown, West Virginia. Progress on this project was also reported (at Honeywell's expense) at the High-Temperature Electronics Network (HiTEN) meeting, held at Oxford, United Kingdom in September 2007 (See Appendix 3).

4.1.8 Task 8: Prepare Phase 1 Final Report

The Phase 1 Final Report [reference 4] was delivered on October 12, 2007. This covers in detail all aspects of the specifications, physical and electrical design of the RPDA module, as well as materials and components to be used, processes for assembly and screening, test considerations, reliability, and risk assessment.

4.2 Phase 2 Results

Phase 2 activity was significantly modified relative to the Research Management Plan [November1]. In order to address issues with the HTEEPROM tasks 16 and 17 were added to the program. These added tasks were performed out of time-sequence relative to the contractual task numbering. Tasks 16 and 17 were performed concurrently with Task 10, and prior to Tasks 11, 12, and 13.

4.2.1 Task 9: MCM Package Procurement

The MCM package design was modified at the beginning of Phase 2 to incorporate an embedded heater within the package[1]. The purpose of the heater is to ensure that the RPDA could be tested at a temperature sufficient to emulate ambient environments of up to 250°C. After the vendor package drawings were updated with this design change, a Critical Design Review (CDR) was completed and packages (and lids) were then procured from Honeywell's MCM package vendor. The order was placed for 100

[1] A patent application was filed with the U.S. Patent Office (application number 12/172317).

packages. However, the package vendor's initial build yielded only 7 4 units, and so the order quantity was adjusted to that quantity at a pro-rated cost. These units were procured to a release Honeywell package drawing, 22030981-001. Figures 4, 5, 6, and 7 are details from that drawing.

Figure 3 is a detail from the assembly drawing that shows the package cavity and internal components, specifying where each component is placed within the cavity. Figure 5 shows the physical dimensions of the package, and Figure 4 is a cross-section showing the stack-up of the routing layers incorporated within the ceramic body of the MCM. Pin placement is shown if Figure 6. The cross section of Figure 4 shows how three layers of ceramic material (and the associated inter-layer signal routing) are removed where capacitors are located. This is done to accommodate the height of the ceramic chip capacitors.

An updated pin list for the RPDA is provided in Table 3, and a map showing the assignment of pins by location is provided in Table 4. Functional definition of the HTFPGA pins is in accordance with those given in reference 5, and definition of the HTSRAM pins are in accordance with those given in reference 8. A description of the HTEEPROM pin functionality is provided in Appendix 2.

Several pin assignments were changed (after the Phase 1 Final Report was issued) in order to accommodate the heater. Those pin assignments that changed are highlighted in Table 3. The MCDAC functional specification (Appendix 1) was also updated with these changes.

The actual routing of the heater is shown in Figure 7. The heater is electrically connected between three pins at one end of the package (C21, D21, and E21) and the VSS plane at the other end of the package. An additional routing layer was added to the package stack-up for the heater, and the heater routing on this layer can be seen as the tungsten interconnect serpentine that runs through the package. It can be seen that the routing is specifically concentrated in those areas directly underneath the SOI IC's. Current passed through the heater (by applying a voltage source to the heater pins while VSS is at 0V) results in Joule heating, which enable high-temperature testing of the device. The heater pins are intended to be left un-connected or else tied off to VSS in an actual application.

4.2.2 Task 10: RPDA Test Hardware and Software

The testing of the prototype assemblies built under this project was performed using automated test equipment (ATE) that is also expected to be the production test environment when the RPDA is commercialized after this project is concluded. This equipment is previously installed and in use at Honeywell's facility in Plymouth, Minnesota.

Multiple test platforms are available, but a Credence 9000 series test platform was chosen for this device. This test platform has capacity for 139 signal pins with bi-directional force/measurement capability. As is usual in the development of package tests on this platform, a custom interface board was designed and procured. In this case the board was ordered specifying high-temperature polyimide circuit board material. A 3M/Textool™ high-temperature PGA socket was placed on the board and soldered in place using a high-melting-point solder.

One limitation of this automated test environment at Honeywell is that maximum test temperature is limited by supporting test equipment. High-temperature package testing is normally done by blowing heated air to the part under test. The maximum control temperature of this air source is 225°C. Due to thermal conduction through the package pins, cabling, and test board the internal die temperature achieved would be significantly less than 225°C. This is the reason that the heater approach was adopted for high-temperature testing.

Test software was prepared to use in this test environment by converting the stimulus/response patterns obtained either from simulation or from previously implemented component testing to test vector files that can be automatically applied by the tester. The overall test strategy consisted in first testing the functionality of the HTEEPROM and HTSRAM while the HTFPGA was held in a state where all of the HTFPGA I/O were in a high-impedance mode (tri-state). Test patterns were then applied and monitored to accomplish loading of the MCDAC configuration file into the HTEEPROM, followed by down-loading of the HTEEPROM configuration into the HTFPGA, and subsequent functional testing to verify functionality of the MCDAC configuration. The scope and content of the tests developed for the RPDA are provided in more detail within the RPDA Characterization Report [reference 8]

4.2.3 Task 16: HTEEPROM Design Verification

This task was added to the project with a SOPO revision early in Phase 2. This was undertaken as a risk reduction that grew into a larger effort than planned. The original risk was due to the fact that the first-pass HTEEPROM die available to this project were obtained from a previous Deep Trek project (Deep Trek High-Temperature Electronics project, DE-FC26-03NT41834). However, there was no design verification testing performed due to insufficient budget under that project. Therefore, this Task 16 was added in order to verify suitability of the HTEEPROM die for meeting the objectives of the RPDA.

The initial approach taken was to assemble and test sample HTEEPROM die. The assembly used an existing package suitable for verification testing. The test plan involved adapting existing test fixtures and boards (previously used to test other memory products) using PC-based test software and general-purpose lab equipment.

Although this was completed, no meaningful results were obtained because the parts were unresponsive. Because the HTEEPROM is such a key element of this project, additional un-planned effort was applied to identify (and correct) the source of the problem. Briefly stated, this involved:

1. Re-inspection of package assembly, board routing, interconnect cabling, and test software;
2. Additional simulation to re-verify expected functionality;
3. Expanding the scope of testing to include additional test-modes and other diagnostic experiments;
4. Identification of means to work around design errors, including identification of Focused-Ion Beam (FIB) repairs;
5. Subsequent additional testing and verification.

This extra effort was successful in the sense that the root cause of the problem was found (two separate inter-connect design/layout errors) and corrective action identified and validated using Focused Ion Beam techniques to "cut and jumper" internal signal routing. This enabled demonstration of the HTEEPROM as reported at the IMAPS High-Temperature Electronics Conference (HiTEC) in May 2008 (Appendix 3). However, this success came at the cost of delays and cost impacts which were addressed by an additional SOPO revision to add Task 17, and make other program adjustments in scope and schedule.

After the HTEEPROM design corrections were implemented by re-design, the HTEEPROM design verification was completed by wafer-level testing of a wafer from the re-design proof-lot. Die from this wafer were used by the program in Task 12.

4.2.4 Task 17: HTEEPROM 2nd Pass Development and Fabrication

A re-design of the HTEEPROM was undertaken in order to correct the design and fabricate die for prototype RPDA assembly and test. In addition, to the two "fatal" design/layout errors identified, other known deficiencies were simultaneously addressed. These resolved issues with HTEEPROM/HTFPGA configuration speed, automatic HTEEPROM memory refresh function, and serial-mode reading. Funding for the required photo-masks was provided by Honeywell at no cost to the program. A proof lot was fabricated. One wafer was split out for use by this project, and verified by wafer probe testing (under task 16). The wafer yielded thirty passing die. Seven of these were consumed in the prototype assembly units that were used in RPDA characterization testing (Task 13). The remaining un-used die from the wafer were not charged to this project and have been retained by Honeywell.

4.2.5 Task 11: Components to Support Assembly of RPDA Prototypes

This task was built into the project WBS in order to collect costs associated with assembling die for the RPDA prototypes. As it turned out, HTSRAM die were obtained from Honeywell catalog inventory; HTFPGA die were obtained as residual material from the previously completed Deep Trek project (DE-FC26-03NT41834), and HTEEPROM die were obtained as a result of Task 17.

4.2.6 Task 12: RPDA Assembly

The object of this task was to assembly prototype RPDA units for characterization testing and to fulfill the deliverable requirement of the program, specifically five units to be delivered to DOE NETL.

Seventy four packages were received from Honeywell's package vendor. Twenty four of these were consumed during first article inspection, development of lid seal process, and development of assembly tooling. One unit was used as a set-up part to validate the correct set-up of wirebond equipment and program.

A prototype lot consisting of seven units was then assembled. The RPDA assembly was completed as Honeywell part number 22031388, with an associated Bill-of-Material released into Honeywell's configuration management system. The units were assembled in accordance with an assembly and screening sequence customized for the RPDA assembly (Honeywell standard flow SF-674, "High Temp RPDA Assembly and

Screen"). An assembly drawing was also prepared and released (Honeywell documents 22031393) to specify component placement within the package and other assembly details. Figure 3 is a detail from that assembly drawing. The prototype units were assembled in accordance with the released wirebond diagram 22020720-001-37AE1. Details from that wirebond diagram are provided as figures 8a through 8d.

One of the seven units was left without sealing the lid. This was done in order to obtain photographs. However, it was tested during characterization (task 13) with the lid temporarily attached by high-temperature tape.

NOTE: Although the Bill-of-Materials specifies the usage of the following high-temperature ceramic chip capacitors:

- Seven 10nF capacitors for HTEEPROM charge pump application
- Two 0.1uF capacitors for analog/digital power supply by-pass/filtering

These were not used. Instead, other capacitors from the same capacitor vendor were used. These other capacitors have the same voltage rating, dimensions, materials, and high-temperature specifications, but they have a different capacitance value. In place of the 10nF capacitors, 22nF capacitors were used. Instead of the 0.1uF capacitors, 0.22uF capacitors were used. The capacitance value is not critical to the RPDA performance, and the substitution was made for convenience.

Note that the forty-two remaining packages that were not consumed have not been charged to this project, and they are retained by Honeywell.

4.2.7 Task 13: RPDA Characterization Testing

Seven characterization units were tested using Automated Test Equipment (ATE) at Honeywell's Aerospace facility in Plymouth, Minnesota. Testing was performed on a LTX-Credence 9000 Series tester. A much more detailed description of the testing performed and the results has been provided within the RPDA Characterization Test Report [reference 9].

The primary objectives of this testing are verification of:

a. Inter-operability of the of the internal components,
b. Correct routing of signals within the MCM package
c. Capability for the MCM to be configured using configuration data stored in the HTEEPROM
d. Demonstration of operation at min/max supply voltage (4.5V to 5.5V) and over a temperature range of -55C to 250C.

Initial testing was completed without using the internal heater and was therefore limited to a temperature range of -55°C and +125°C. The first attempt at using the heater led to an accident resulting in deformation (partial melting) of the test socket. This event coincided with the end of the project period of performance. That being the case, five units were shipped to DoE/NETL to satisfy the deliverable requirements of this project. Since then (at Honeywell expense) the socket was replaced and the test board has been repaired so that additional testing of two units could be completed at up to 250°C and the results noted in the Characterization Test Report.

The results of this testing were successful in meeting the test objectives. The results are provided in more detail within the Characterization Report. Three units passed all tests under all conditions under which they were tested (up to 125°C). One unit passed all tests under all conditions from -55°C to 225°C. The same unit passed most tests at 250°C as well. Based on these results, conclusions are

- The RPDA package meets the electrical connectivity requirements for the RPDA package.
- Capability has been shown to independently validate the HTEEPROM and HTSRAM die after they have been assembled within the RPDA package.
- Capability has been shown for operation of the HTEEPROM (both read and write) over the full temperature range and supply conditions.
- It has been demonstrated that data loaded into the HTEEPROM can be accessed and down-loaded into the HTFPGA in order to configure the RPDA for the functionality intended by the user.
- It has been demonstrated by exercising the RPDA configured as a Multi-Channel Data Acquisition Controller (MCDAC) that the FPGA is able to read and write data to the SRAM within the RPDA in a functional configuration.
- I/O parametric test results have been obtained that may be used to establish design and screening criteria for future applications.
- The embedded heating element has demonstrated as capable for achieving elevated test temperatures (above 250C) within a test system otherwise developed for conventional (-55C to 125C) temperature testing.

Additional work would be required in order to fully identify the cause of failures that occurred in some units under some test conditions. However, the most likely causes could be addressed by a combination of improved component screening, adjustment of test pattern timing, and/or an assembly and screening flow that allows for component rework. These are topics for additional development and commercialization activity after this project is complete.

4.2.8 Task 14: RPDA Life-test and Report (Removed)

This task was originally included in the project, with the objective of completing a high-temperature 1000-hour powered life-test of RPDA prototypes. It was removed from the project in order to partially compensate for the funding of added Tasks 16 and 17.

4.2.9 Task 15: Phase 2 Program Support

Program support has been provided monitoring and reporting of financial and technical progress, and adjustment of project plans (including SOPO revisions) are required. Deliverable technical, financial, and administrative reports have been generated.

5.0 Conclusions

The objective of this project has been the specification, design, prototype fabrication and testing of a High-temperature, re-programmable electronics module that can be configured to provide a wide range of digital functions in a package suitable for down-hole oil and gas exploration tools and production well monitoring. The project is now complete, and has succeeded in meeting almost all of the objectives that it was it set out to meet. This has been achieved by the development of the Reconfigurable Processor for Data Acquisition (RPDA)

MCM. This module incorporates high-density signal routing embedded within a rugged, high-temperature ceramic package. This is combined it with High-temperature Silicon-on-Insulator (SOI) electronics with an extraordinarily wide operating temperature range. Programmability for a wide range of functionality is achieved by the selection of SOI integrated circuits, which include non-volatile High-temperature EEPROM, Field Programmable Gate Array, and SRAM. Prototypes of this module have been assembled, tested, and delivered. The MCM design, components, materials, and construction all are suitable for long-term reliable operation at a temperature of 225°C and above in a form factor suitable for the intended application. Furthermore, this project has demonstrated configuration of this device as a Multi-Channel Data Acquisition Controller. While this is useful on its own merit, it also serves to demonstrate and verify the feasibility for the configuration tools and software.

The RPDA addresses a unique, previously unfilled need for flexible, re-programmable digital electronics that can be used in the extreme environments required for down-hole oil and gas drilling, exploration and production.

In addition to development of the MCM package, this project has resulted in the completion of the development and prototype demonstration of a complete, functional High-temperature EEPROM, capable of performance (both read/write) at 250°C. This result is equally significant to the industry and high-temperature electronics community as the development of the RPDA itself. Industrial interest is reflected in the acceptance of technical papers and presentations at HiTEN 2007 and HiTEC 2008.

As a result of this project, the RPDA and HTEEPROM both are positioned for the establishment of final specifications and manufacturing test development, leading to commercial offering and availability of these components for the oil and gas industry, as well as other extreme temperature applications.

Table 1: RPDA Recommended Operating Conditions

Parameter	Limits			Units
	Min	Typical	Max	
Positive Supply Voltage	**4.75**	**5.0**	**5.25**	**Volts**
Voltage On Any Pin (1)	**-0.3**		**V_{DD}+0.3**	**Volts**
Capacitive Output Load			**TBD**	**pF**
Case Operating Temperature	**-55**		**225**	**°C**

(1) TM_VP and TM_VM pins are exceptions when data is being written to the HTEEPROM (these pins are listed in Table 3 as package pins D19 and D17 respectively). These pins are connected to the HTEEPROM internal charge-pumps and will typically be at +8.5V (VP) and -8.5V (VSS) during HTEEPROM write operations. Otherwise, during normal operation they are constrained to the voltages in the above table.

Table 2 - Absolute Maximum Specifications

Symbol	Parameter	Ratings(1)		Units
		Min	Max	
V_{DD}	Positive Supply Voltage (2)	-0.5	6.5	Volts
VPIN	Voltage on Any Pin (2, 5)	-0.5	V_{DD} + 0.5	Volts
IOUT	Average Output Current	-20	20	mA
TSTORE	Storage Temperature	-65	250	°C
TSOLDER	Soldering Temperature (5 seconds)		355	°C
P_D	Package Power Dissipation (3)		3	W
$Ø_{JC}$	Package Thermal Resistance 147 PGA MCM (Junction to Case)		7.0	°C/W
VPROT	Electrostatic Discharge Protection Voltage (4)	2000		V
T_J	Junction Temperature		300	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.

(2) Voltage referenced to V_{SS}

(3) RPDA power dissipation due to I_{DDS}, I_{DDOP}, and I_{DDSEI}, plus RPDA output driver power dissipation due to external loading must not exceed this specification

(4) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015. This is goal. ESD withstand capability has not been established for all of the components (as of Jan. 31, 2007).

(5) VP and VM test pins are exceptions when data is being written to the HTEEPROM. These pins are connected to the HTEEPROM internal charge-pumps and will typically be at +8.5V (VP) and -8.5V (VSS) during HTEEPROM write operations. Otherwise, during normal operation they are constrained to the voltages in the above table.

Table 3- RPDA Package Pin Functions and Internal Connections

Package Pin	Signal Name	HTFPGA Connection	HTFPGA Dual Function	HTSRAM Connection	HTEEPROM Connection	Function
A1	VDD	VDD		VDD	VDD	Power
A2	VSS	VSS		VSS	VSS	Ground
A3	SR_NOE	IO_204		NOE		HT6256 SRAM Output Enable
A4	SR_NCS	IO_198		NCS		HT6256 SRAM Chip Select
A5	IO_1	IO_1				
A6	IO_5	IO_5				
A7	IO_11	IO_11				
A8	IO_17	IO_17				HTFPGA Programmable I/O
A9	IO_26	IO_26				
A10	IO_33	IO_33				
A11	IO_39	IO_39				
A12	M0	M0				HTFPGA Configuration Control
A13	CLOCK	CLOCK				HTFPGA Core Clock
A14	RESETN	RESETN			POROUTN	HTEEPROM Power-on Reset Out / HTFPGA Reset In
A15	EE_NRFSHRQ	IO_53			NRFSHRQ	HTEEPROM Refresh Request
A16	EE_NRFSHACK	IO_54			NRFSHACK	HTEEPROM Refresh Acknowledge
A17	EE_A2	IO_58			A2	
A18	EE_A5	IO_62			A5	HTEEPROM Parallel Address
A19	EE_A8	IO_66			A8	
A20	VSSA				VSSA	HTEEPROM Analog Ground
A21	VDDA				VDDA	HTEEPROM Analog Power
B1	SR_NWE	IO_184		NWE		HT6256 SRAM Write Enable
B2	SR_A8	IO_192		A8		
B3	SR_A11	IO_200		A11		HT6256 SRAM Address
B4	SR_A10	IO_202		A10		
B5	SR_D7	IO_194		D7		HT6256 SRAM Data
B6	IO_7	IO_7				
B7	IO_13	IO_13				
B8	IO_19	IO_19				HTFPGA Programmable I/O
B9	IO_27	IO_27				
B10	IO_35	IO_35				
B11	IO_41	IO_41				
B12	M2	M2				HTFPGA Configuration Control
B13	M1	M1				
B14	IO_51	IO_51				HTFPGA Programmable I/O
B15	EE_A1	IO_57	A1		A1	
B16	EE_A3	IO_60	A3		A3	
B17	EE_A6	IO_64	A6		A6	HTEEPROM Parallel Address
B18	EE_A9	IO_68	A9		A9	
B19	EE_A11	IO_70	A11		A11	
B20	EE_A13	IO_73	A13		A13	
B21	EE_D7	IO_89	D7		D7	HTEEPROM Parallel Data

Table 3- RPDA Package Pin Functions and Internal Connections (Continued)

Package Pin	Signal Name	HTFPGA Connection	HTFPGA Dual Function	HTSRAM Connection	HTEEPROM Connection	Function
C1	SR_A14	IO_180		A14		HT6256 SRAM Address
C2	SR_A13	IO_188		A13		
C3	SR_A9	IO_196		A9		
C4	SR_D6	IO_190		D6		HT6256 SRAM Data
C5	SR_D5	IO_186		D5		
C6	IO_9	IO_9				HTFPGA Programmable I/O
C7	IO_15	IO_15				
C8	IO_21	IO_21				
C9	IO_29	IO_29				
C10	IO_37	IO_37				
C11	IO_43	IO_43				
C12	IO_45	IO_45				
C13	IO_47	IO_47				
C14	IO_49	IO_49				
C15	EE_A4	IO_61	A4		A4	HTEEPROM Parallel Address
C16	EE_A7	IO_65	A7		A7	
C17	EE_A10	IO_69	A10		A10	
C18	EE_A12	IO_72	A12		A12	
C19	EE_A14	IO_74	A14		A14	
C20	EE_D6	IO_86	D6		D6	HTEEPROM Parallel Data
C21	HEATER					Heater
D1	SR_A12	IO_174		A12		HT6256 SRAM Address
D2	SR_A5	IO_162		A5		
D3	SR_D4	IO_182		D4		HT6256 SRAM Data
D4	SR_D3	IO_178		D3		
D5	IO_145	IO_145				HTFPGA Programmable I/O
D6	IO_137	IO_137				
D7	IO_129	IO_129				
D8	IO_23	IO_23				
D9	IO_31	IO_31				
D10	IO_109	IO_109				
D11	IO_101	IO_101				
D12	IO_100	IO_100				
D13	IO_90	IO_90	TESTCLK			HTFPGA Programmable I/O
D14	EE_A0	IO_56	A0		A0	HTEEPROM Parallel Address
D15	TM_NRFSHOSC/ TM_ECC_NDISABLE				TM_NRFSHOSC/ TM_ECC_NDISABLE	HTEEPROM Test Pin
D16	TM_NPOE_NRFSHDIV				TM_NPOE/ TM_NRFSHDIV	
D17	TM_VM				TM_VM	
D18	TM_NSELHLF				TM_NSELHLF	
D19	TM_VP				TM_VP	
D20	TMPDIODE				TMPDIODE	
D21	HEATER					Heater

Table 3- RPDA Package Pin Functions and Internal Connections (Continued)

Package Pin	Signal Name	HTFPGA Connection	HTFPGA Dual Function	HTSRAM Connection	HTEEPROM Connection	Function
E1	SR_A7	IO_170		A7		HT6256 SRAM Address
E2	SR_A3	IO_154		A3		
E3	SR_D2	IO_176		D2		HT6256 SRAM Data
E4	SR_D1	IO_172		D1		
E5	IO_147	IO_147				HTFPGA Programmable I/O
E6	IO_139	IO_139				
E7	IO_131	IO_131				
E8	IO_123	IO_123				
E9	IO_117	IO_117				
E10	IO_111	IO_111				
E11	IO_103	IO_103				
E12	IO_98	IO_98				
E13	IO_92	IO_92	CENFG			HTFPGA Configuration Control
E14	EE_CSN	IO_77	A16		CSN	HTEEPROM Chip Select
E15	EE_D0	IO_80	D0		D0	HTEEPROM Parallel Data
E16	EE_D1	IO_81	D1		D1	
E17	EE_D2	IO_82	D2		D2	
E18	EE_D3	IO_84	D3		D3	
E19	EE_D4	IO_85	D4		D4	
E20	EE_D5	IO_86	D5		D5	
E21	HEATER					Heater
F1	SR_A6	IO_166		A6		HT6256 SRAM Address
F2	SR_A4	IO_158		A4		
F3	SR_D0	IO_168		D0		HT6256 SRAM Data
F4	SR_A0	IO_164		A0		HT6256 SRAM Address
F5	IO_149	IO_149				HTFPGA Programmable I/O
F6	IO_141	IO_141				
F7	IO_133	IO_133				
F8	IO_125	IO_125				
F9	IO_119	IO_119				
F10	IO_113	IO_113				
F11	IO_105	IO_105				
F12	CSOUT	CSOUT	CSOUT			HTFPGA Configuration Control
F13	EE_CFG_PROT				CFG_PROT	HTEEPROM Configuration Protect Pin
F14	EE_WEN	IO_75			WEN	HTEEPROM Write Enable
F15	EE_SELSNP				SELSNP	HTEEPROM Parallel/Serial Configuration Control
F16	EE_SI				SI	HTEEPROM Serial Input
F17	EE_HOLDN				HOLDN	HTEEPROM Serial Hold Pin
F18	EE_SBP1				SBP1	HTEEPROM Serial Block Protect Pin
F19	CHECKN	CHECKN	CHECKN		CHECKN	HTFPGA Configuration Control
F20	CONN	CONN			CONN	
F21	POROUTN	POROUTN			PORINN	HTFPGA Power-on Reset Out/ HTEEPROM Power-on-Reset In

Table 3- RPDA Package Pin Functions and Internal Connections (Continued)

Package Pin	Signal Name	HTFPGA Connection	HTFPGA Dual Function	HTSRAM Connection	HTEEPROM Connection	Function
G1	VDD	VDD		VDD	VDD	Power
G2	VSS	VSS		VSS	VSS	Ground
G3	SR_A1	IO_150		A1		HT6256 SRAM Address
G4	SR_A2	IO_156		A2		
G5	IO_151	IO_151				HTFPGA Programmable I/O
G6	IO_143	IO_143				
G7	IO_135	IO_135				
G8	IO_127	IO_127				
G9	IO_121	IO_121				
G10	IO_115	IO_115				
G11	IO_107	IO_107				
G12	UNRSTN	UNRSTN				Auxilliary HTFPGA Reset
G13	EE_OEN	IO_76	A15		OEN	HTEEPROM Output Enable
G14	ERRN	ERRN	ERRN		ERRN	HTFPGA Configuration Control
G15	EE_SCK				SCK	HTEEPROM Serial Clock
G16	EE_WPN				WPN	HTEEPROM Serial Write Protect Pin
G17	EE_SBP0				SBP0	HTEEPROM Block Protect Pin
G18	EE_SO				SO	HTEEPROM Serial Data Out
G19	CCLK	CCLK			CCLK	HTFPGA Configuration Clock
G20	VSS	VSS		VSS	VSS	Ground
G21	VDD	VDD		VDD	VDD	Power

Table 4: Package Pin Location Map

KEY

- Power
- Ground
- SRAM/FPGA Common Connection
- FPGA Configurable IO
- FPGA Control Signals
- EEPROM/FPGA Common Connection
- EEPROM Only
- Heater Pin

	A	B	C	D	E	F	G
1	VDD	SR NWE	SR_A14	SR_A12	SR_A7	SR_A6	VDD
2	VSS	SR_A8	SR_A13	SR_A5	SR_A3	SR_A4	VSS
3	SR_NOE	SR_A11	SR_A9	SR_D4	SR_D2	SR_D0	SR_A1
4	SR_NCS	SR_A10	SR_D6	SR_D3	SR_D1	SR_A0	SR_A2
5	IO_1	SR_D7	SR_D5	IO_145	IO_147	IO_149	IO_151
6	IO_5	IO_7	IO_9	IO_137	IO_139	IO_141	IO_143
7	IO_11	IO_13	IO_15	IO_129	IO_131	IO_133	IO_135
8	IO_17	IO_19	IO_21	IO_23	IO_123	IO_125	IO_127
9	IO_26	IO_27	IO_29	IO_31	IO_117	IO_119	IO_121
10	IO_33	IO_35	IO_37	IO_109	IO_111	I)_113	IO_115
11	IO_39	IO_41	IO_43	IO_101	IO_103	IO_105	IO_107
12	M0	M2	IO_45	IO_100	IO_98	CSOUT	UNRSTN
13	CLOCK	M1	IO_47	IO_90	IO_92	EE CFG_PROT	EE_OEN
14	RESETN	IO_51	IO_49	EE_A0	EE_CSN	EE_WEN	ERRN
15	EE NRFSHRQ	EE_A1	EE_A4	TM ECC NDISABLE NRFSHOSC	EE_D0	EE SELSNP	EE_SCK
16	EE NRFSHACK	EE_A3	EE_A7	TM NPOE NRFSHDIV	EE_D1	EE_SI	EE_WPN
17	EE_A2	EE_A6	EE_A10	TM_VM	EE_D2	EE HOLDN	EE_SBP 0
18	EE_A5	EE_A9	EE_A12	TM NSELHLF	EE_D3	EE_SBP1	EE_SO
19	EE_A8	EE_A11	EE_A14	TM_VP	EE_D4	CHECKN	CCLK
20	VSSA	EE_A13	EE_D6	TMPDIODE	EE_D5	CONN	VSS
21	VDDA	EE_D7	HEATER	HEATER	HEATER	POROUTN	VDD

Figure 2: RPDA Functional Block Diagram

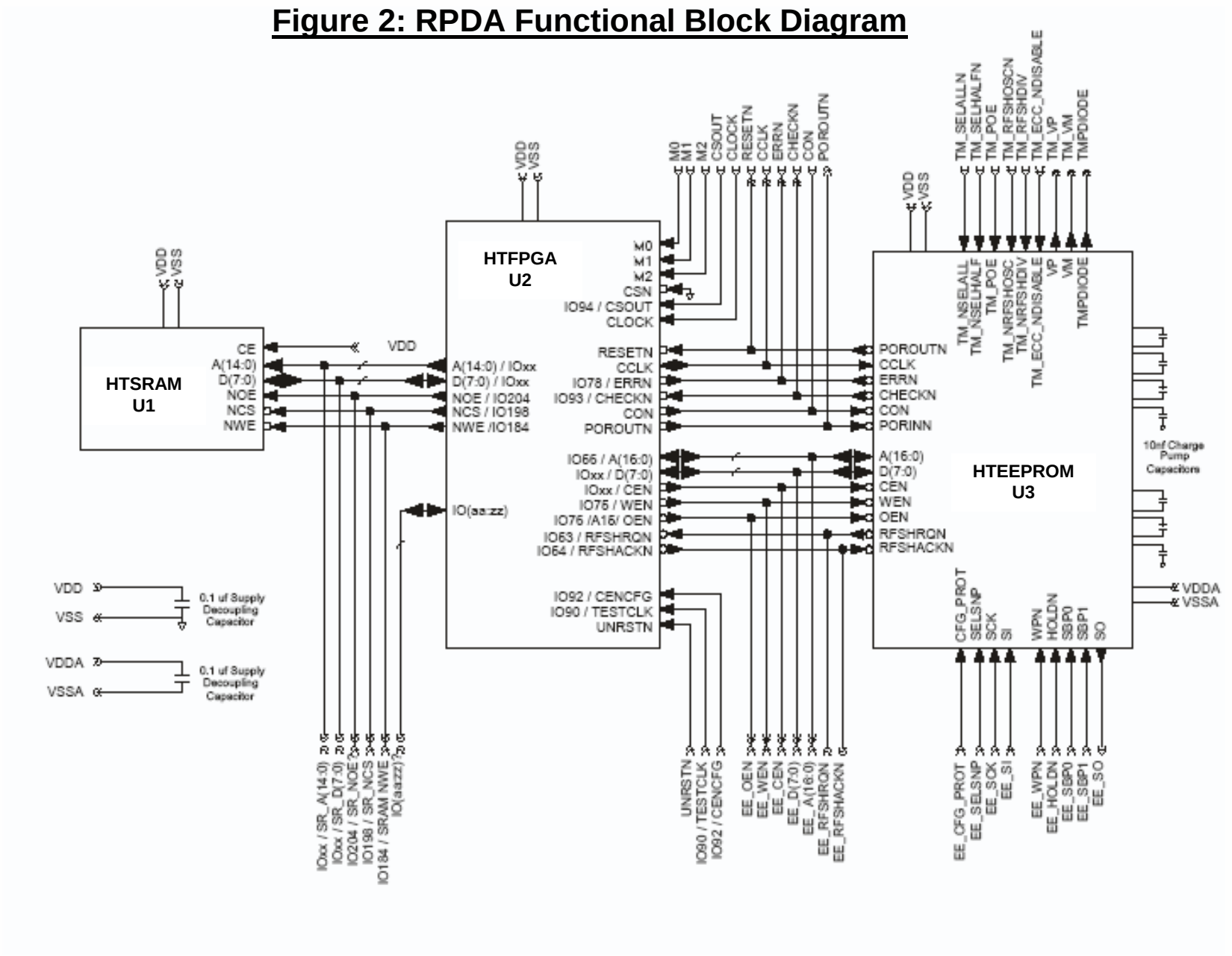
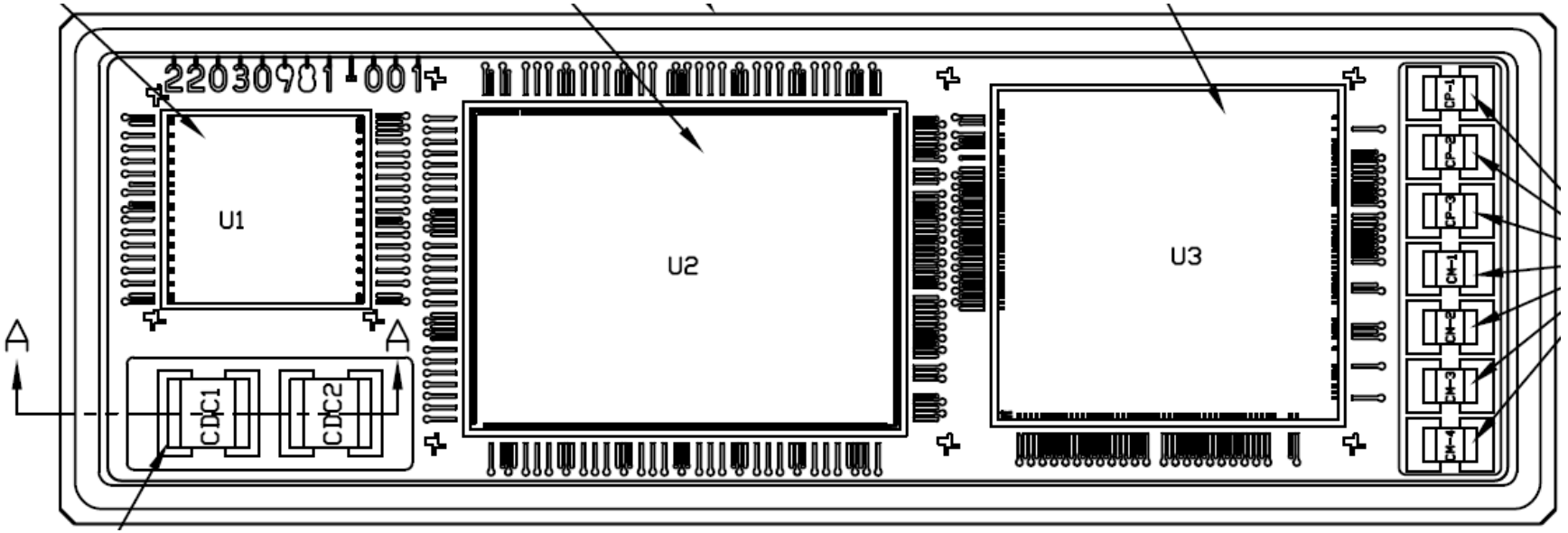


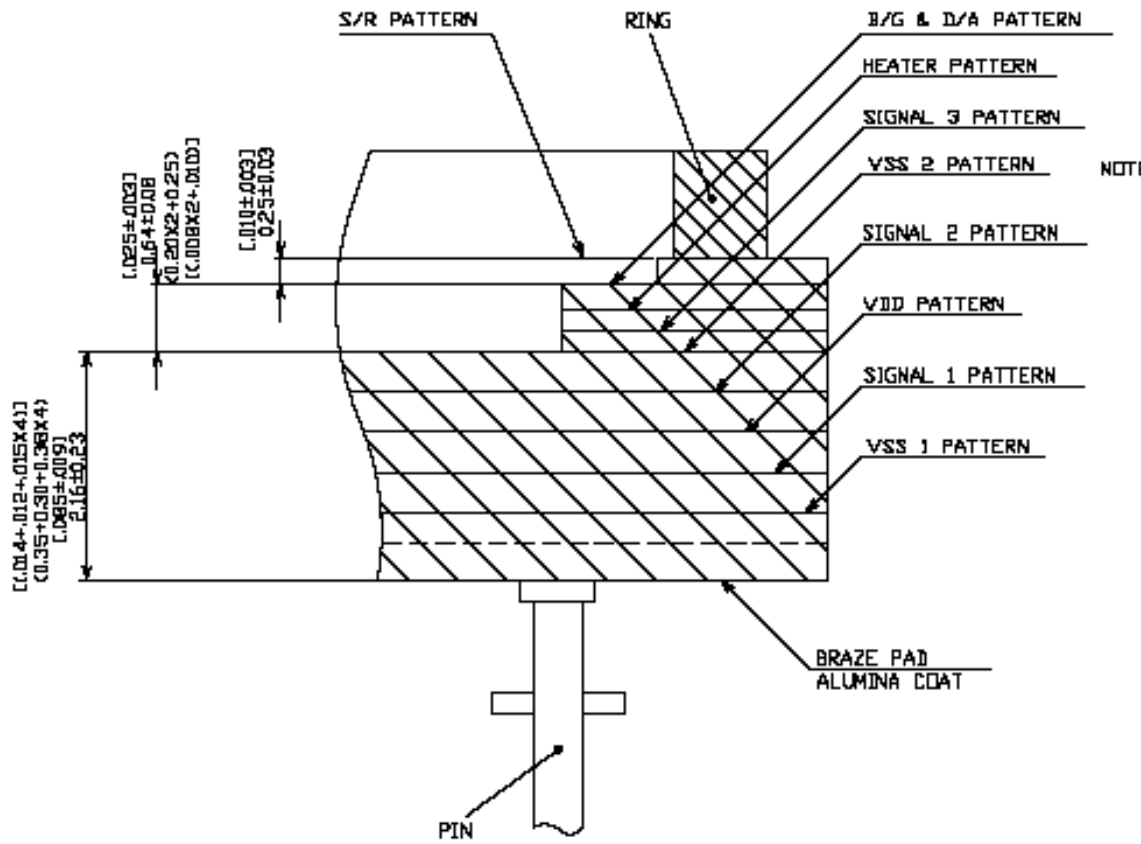
Figure 3: Detail from RPDA Assembly Drawing



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REMARKS	ITEM NO.
1	34168	22030981-001	147 PIN CERAMIC PGA, MCM		9
1	34168	22007791-022	LID, STEP LID, 1.056 X .825 X .020		8
A/R	34168	58032637-001	NON-CONDUCTIVE EPOXY		7
A/R	34168	58032636-001	CONDUCTIVE EPOXY		6
7	34168	22022164-034	HIGH TEMP CAPACITOR, 0805, 10 nF	CN-1, CN-2, CN-3, CN-4, CP-1, CP-2, CP-3	5
2	34168	22022164-033	HIGH TEMP CAPACITOR, 1210, 0.1 uF	CDC1, CDC2	4
1	34168	22030903-XXX	DIE, HIGH TEMP 32KX8 EEPROMM	U3	3*
1	34168	22027498-XXX	DIE, HTFPGA	U2	2*
1	34168	22019256-XXX	DIE, HIGH TEMP 32KX8 SRAM	U1	1*

* COMPONENT TAB NUMBER TO BE SPECIFIED BY PARTS LIST.

Figure 4: MCM Layers



NOTES:

1. ELECTROLESS GOLD PLATE 1.5~5.7㎛[60~225㎲ INCHES] OVER 2.0~8.9㎛[80~350㎲ INCHES] ELECTROLESS NICKEL.
2. S/R AND D/A TO BE ELECTRICALLY CONNECTED TO VSS.
3. HONEYWELL SPEC 22005260 SHALL APPLY.
4. EXPOSED VIA SHALL BE ALLOWED AT 0.05MAX.
5. HEATER RESISTANCE : 5.3Ω±30%(TARGET). (PIN A2 TO PIN D21)

Figure 5: MCM Package Physical Dimensions

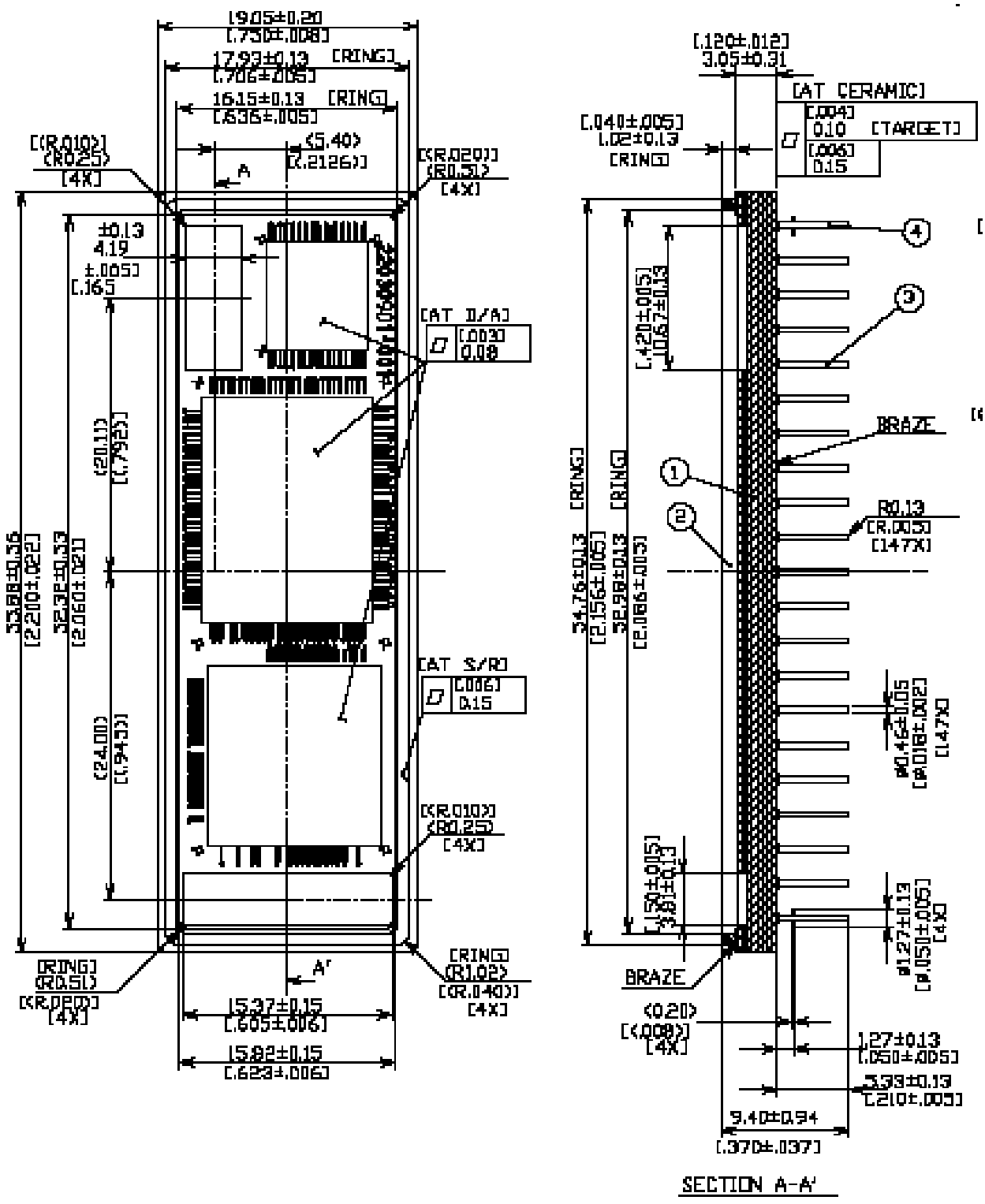


Figure 6: MCM Package Pin Locations

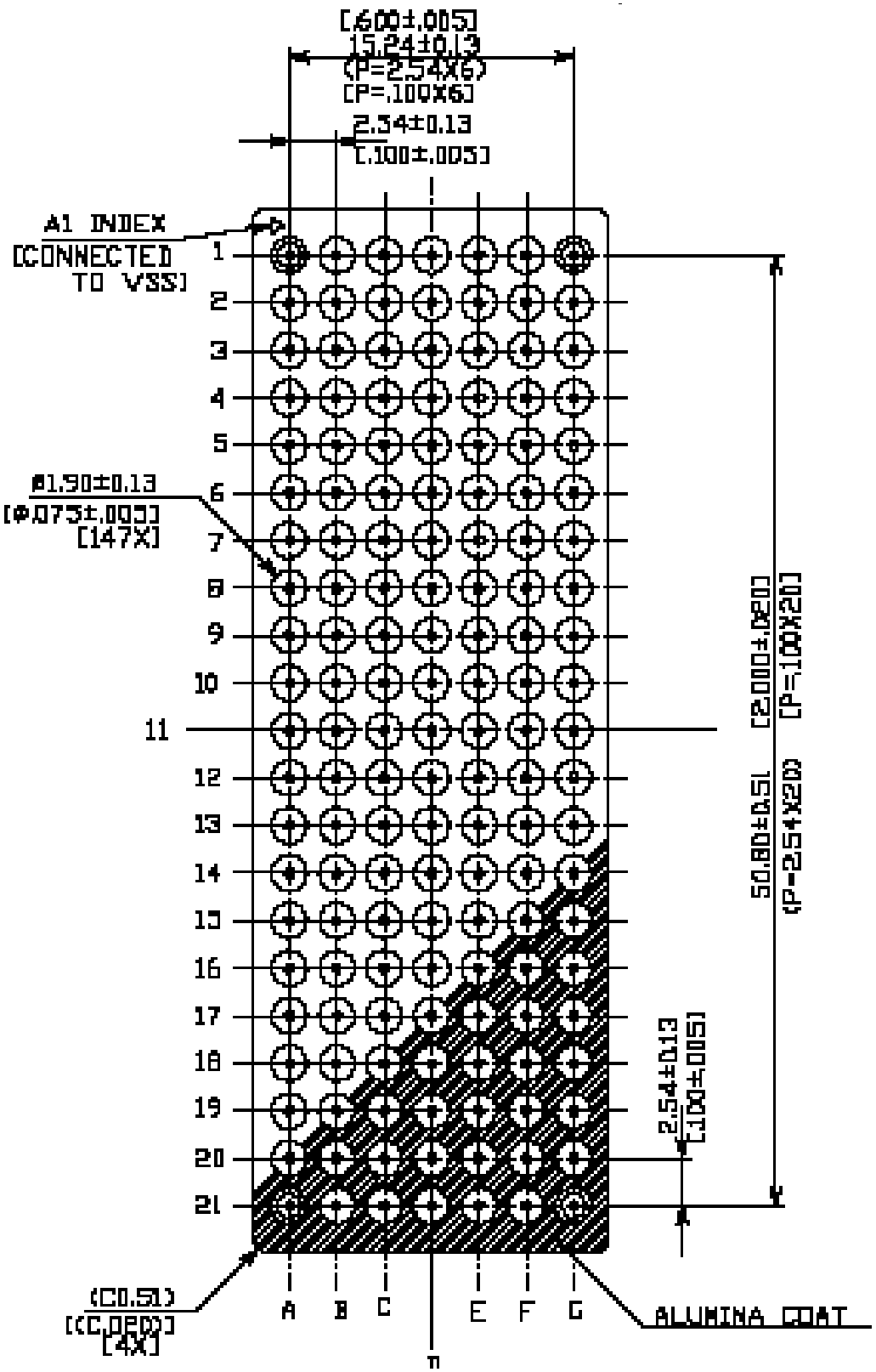


Figure 7: Heater Routing

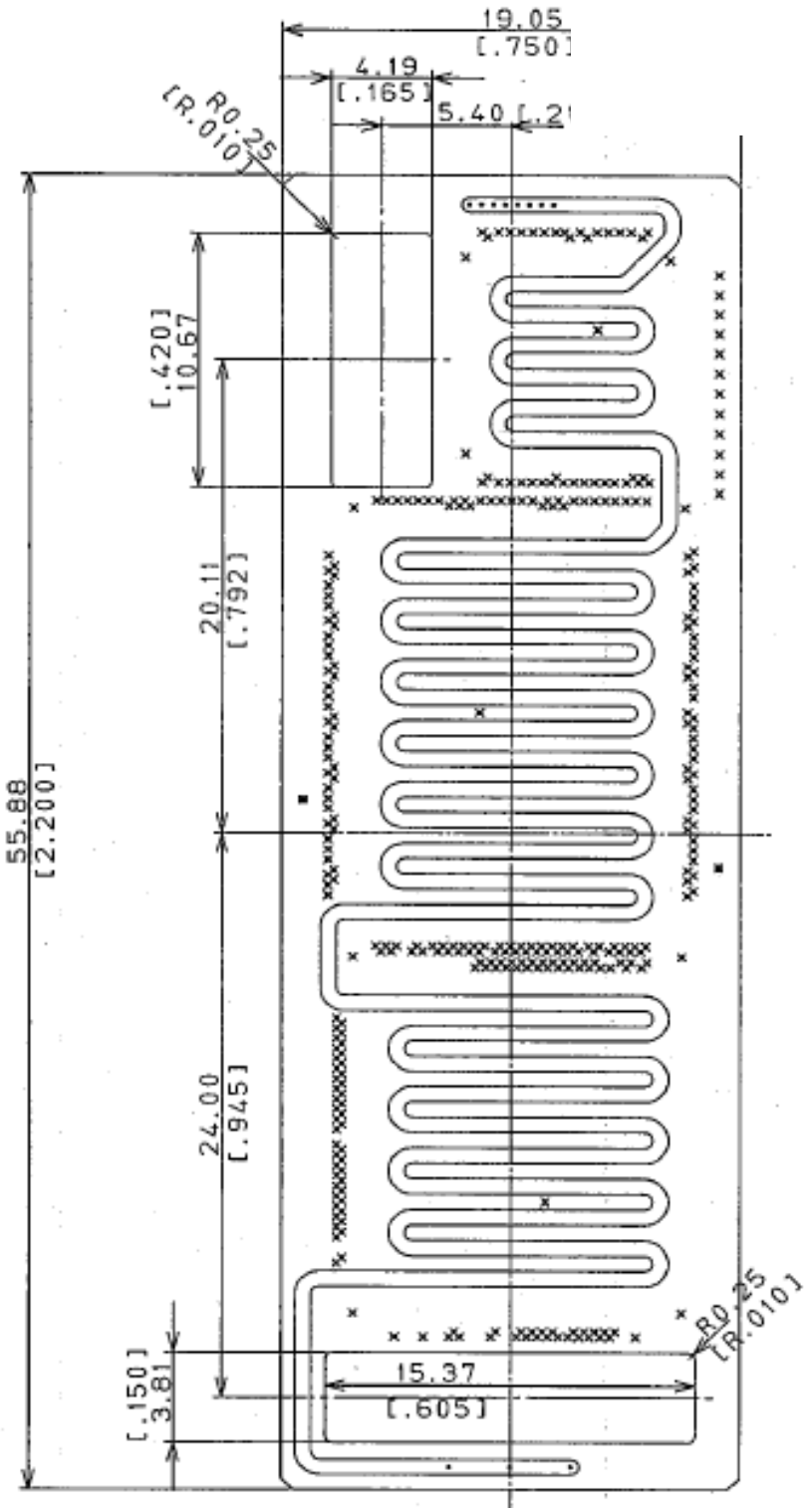
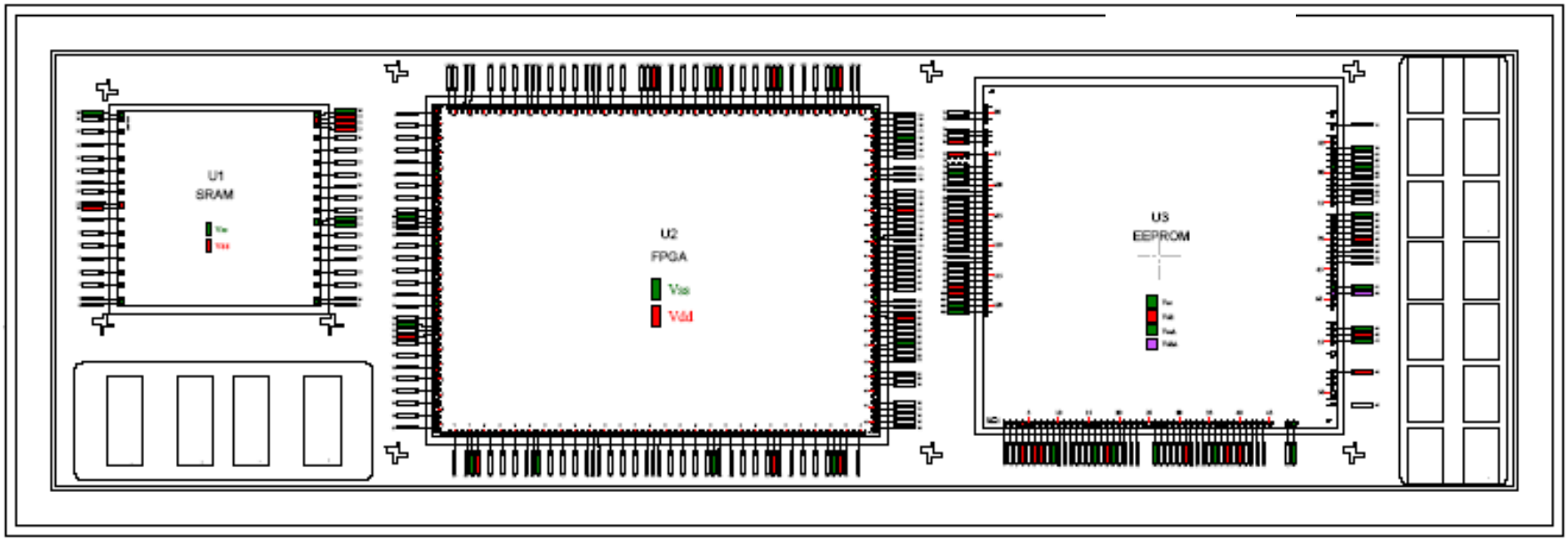
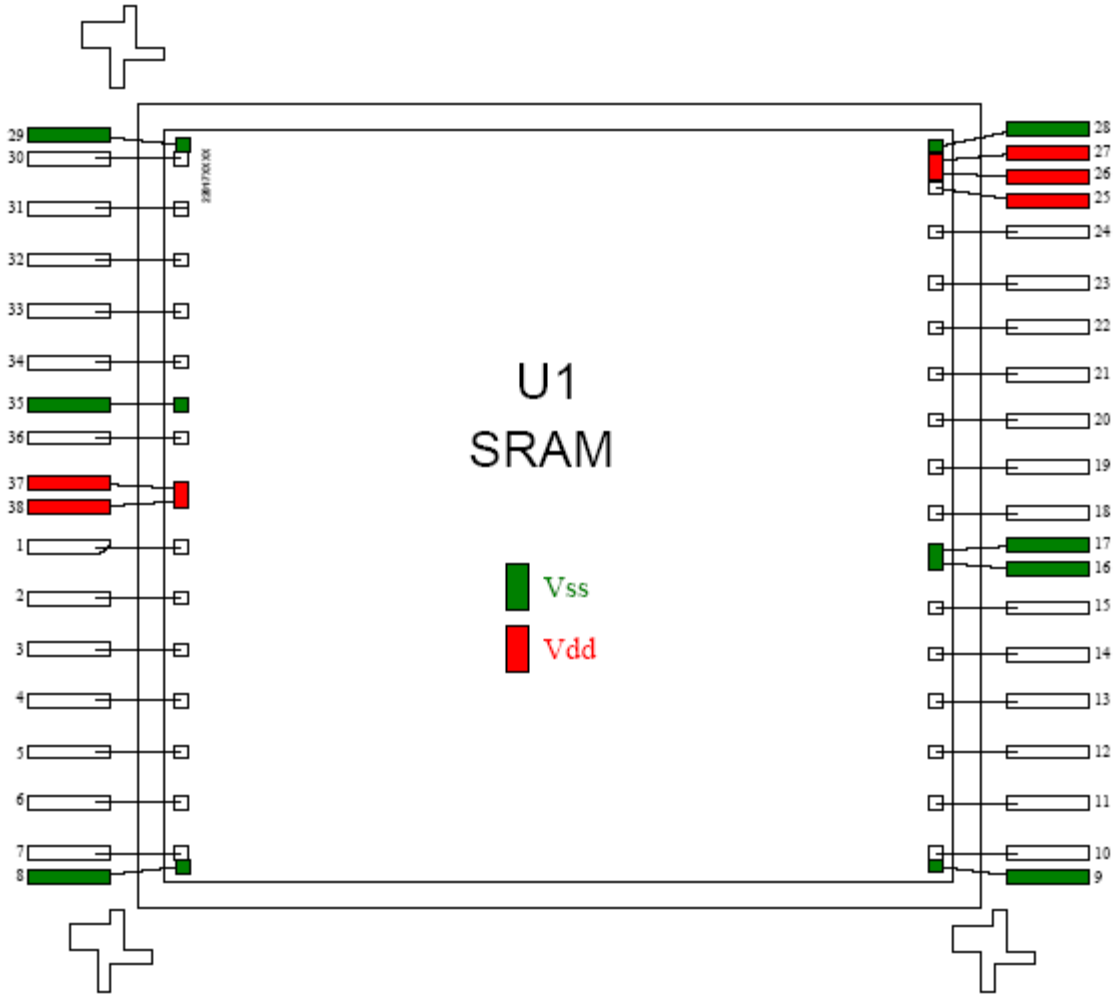


Figure 8a: RPDA Wirebond Diagram



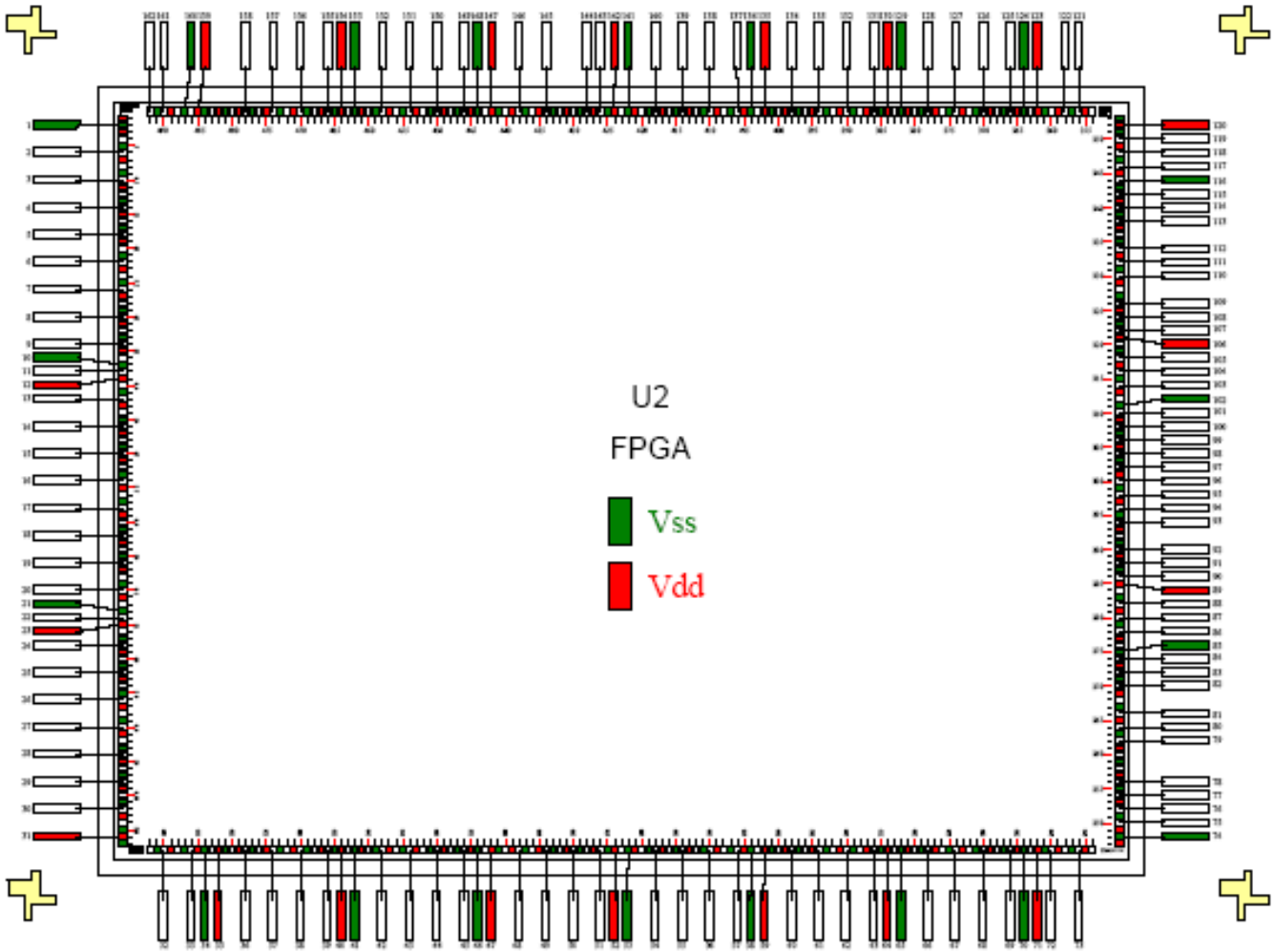
Wire Bond Diagram: rpda_147pga_30981_w001
- Device: RPDA Hi Temp MCM
- Package: 147 pin grid array package

Figure 8b: HT6256 SRAM Component Pad Locations and Wire-bonding



Wire Bond Diagram: rpda_147pga_30981_w001_u1
• Detail of U1

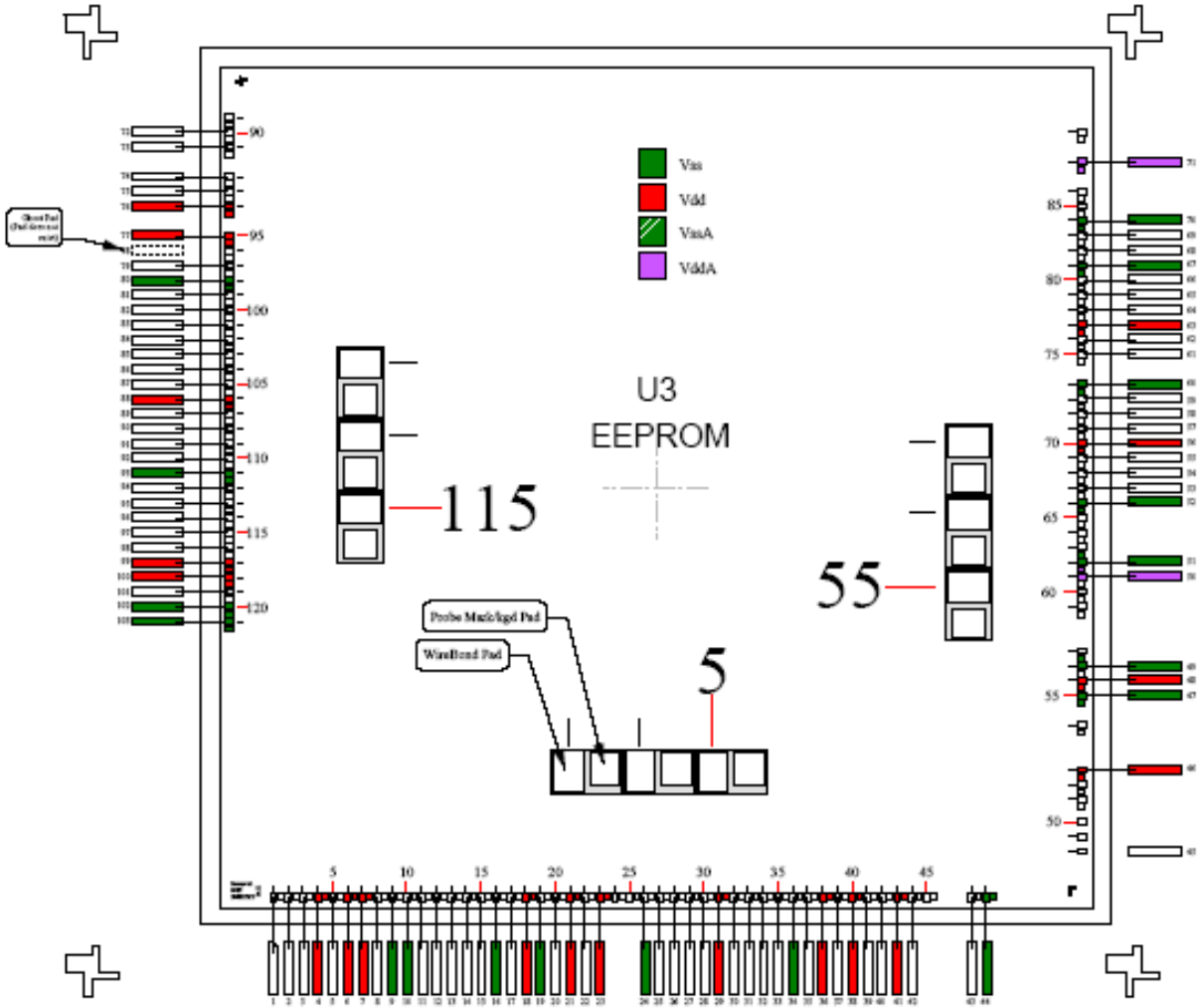
Figure 8c: HTFPGA Component Pad Locations and Wire-bonding



Wire Bond Diagram: rpda_147pga_30981_w001_u2

- Detail of U2

Figure 8d: HTEEPROM Component Pad Locations and Wire-bonding



Wire Bond Diagram: rpda_147pga_30981_w001_u3
- Detail of U3

High Temperature Multi-Channel Data Acquisition Controller
Design Specification

APPENDIX 1 to
Final Report

Deep Trek
Re-configurable Processor for Data Acquisition (RPDA)

Revision 1.01
24 September 2009

Author:
Mike Johnson

Honeywell

Revision History

Revision	Description	Date	By
1.0	Original : Published as Appendix to Final Report of Phase 1: RPDA Phase1 Final Report	12-Oct-2007	Mike Johnson
1.01	Updated Pin-out (Table 8) and MCDAD Signal Map (Table 11) to reflect the addition of the Heater input on pins C21, D21, and E21 plus other HTEEPROM test-pin changes. Corrected pin assignment for pins B12 and B14 in Tables 8 and 11. Modified note to Table 5 Published as Appendix to RPDA Final Report	24-Sep-2009	Bruce Ohme

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1 Introduction

1.1 Overview

This Multi-Channel Data Acquisition Controller (MCDAC) design provides a high temperature module to control and record up to 8-channels of analog data when used in concert with Honeywell's HTADC18 High Temperature 18-bit Analog-to-Digital Converter (ADC) and Honeywell's HT507 High Temperature 8-Channel Analog Multiplexer (AMUX). This design is implemented using the Reconfigurable Processor for Data Acquisition (RPDA).

1.2 Device Description

The MCDAC is built on Honeywell's high temperature Reconfigurable Processor for Data Acquisition (RPDA) platform [1]. This is a multi-chip module (MCM) containing three Honeywell High Temperature products: a field programmable gate array HTFPGA, an HT28C256 EEPROM containing the boot code for the HTFPGA and an HT6256 32Kx8 SRAM. This design is targeted for autonomous and semi-autonomous data logging functions as might be used in deep well measurement while drilling (MWD) and data logging operations.

The MCDAC is organized around a controller/scheduler function that provides data sampling at regular schedules of an external ADC/AMUX combination. Scheduling of measurements is based on programming of external pins. Autonomous measurements occur based on an internal timer derived from the primary SYSCLOCK, which starts the measurement/logging function. Alternatively, measurement on demand can be programmed to occur whenever the SAMPLE_NOW signal is asserted. From one to eight analog channels can be selected for data logging based upon the state of the CHANNEL_SEL bus.

An ADC/AMUX interface function directly controls the external HTADC18 [2], providing wake, measure, and sleep commands through the ADC four-wire Serial Peripheral Interface (SPI) pins, to the HTADC18's 18-bit and 8-bit converters. The ADC/AMUX function also directly controls the address and enable pins of an HT507 [3] analog multiplexer, to steer up to eight channels of analog signals to the front end of the HTADC18.

A First-In/First-Out (FIFO) function is included which takes each 8-bit and 18-bit measurement and stores them along with health and status information into a 32-bit word. Up to 8192 32-bit words can be logged by the on-board memory.

An industry standard SPI interface is used for data transfer to and from the MCDAC at data rates up to 1MHz. The SPI bus is activated through a chip select, enabling communication via the SPI Data In and SPI Data Out pins. Through this interface several operations can occur: the HTADC18 can be put into active and sleep modes, the FIFO data can be downloaded, or most recent measurement data can be downloaded.

2 High Level Description

2.1 Functional Description

The MCDAC is a multi-chip module (MCM) containing a High Temperature Field Programmable Gate Array (HTFPGA), a High Temperature 32Kx8 Static RAM (HTSRAM) and a High Temperature 32Kx8 EEPROM. For this MCDAC design the HTFPGA is configured to control an eight channel High Temperature Analog MUX and an 18-Bit High Temperature Analog-to-Digital Converter. The HTEEPROM is only used as a boot ROM which contains the programming for the HTFPGA. The HTSRAM is used as data storage space in the form of an 8K by 32-bit FIFO. The MCDAC can be programmed through external pin selection to perform autonomous measurements of 1 to 8 channels of analog data, and a schedule that can be selected to perform sampling from once every second to sampling every 19.3 hours. The sampled data is stored in the 8Kx32 FIFO register, which can be unloaded through the slave serial port interface (SPI).

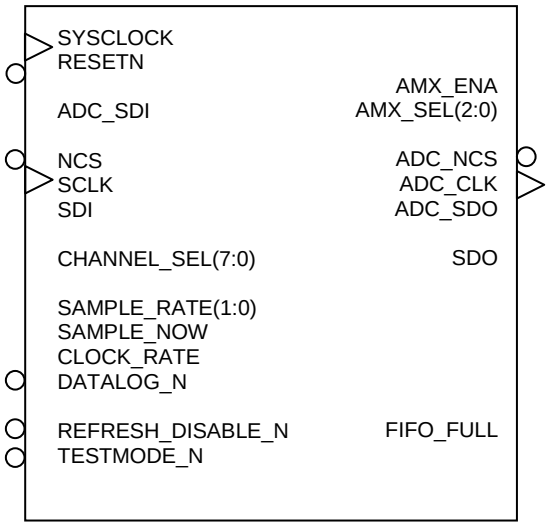


Figure 1 - MCDAC Symbol

Figure 1 shows in symbol format the primary IO. Table 1 gives a brief description of the MCDAC functional pins. Additional pins associated with the generic RPDA module are described in Table 7.

Table 1 - Functional Pin Description

Signal	Type	Function
SYSCLOCK	IN	1MHz Module Clock
RESETN	IN	Global Reset
ADC_NCS	OUT	ADC SPI Chip Select
ADC_CLK	OUT	ADC SPI Clock
ADC_SDO	OUT	ADC SPI Serial Data Out
ADC_SDI	IN	ADC SPI Data In
NCS	IN	SPI Slave Chip Select
SCLK	IN	SPI Slave Clock
SDI	IN	SPI Slave Serial Data In
SDO	OUT	SPI Slave Serial Data Out
CHANNEL_SEL(7:0)	IN	Analog Channel Mask Pins
SAMPLE_RATE(1:0)	IN	Autonomous Sample Rate
SAMPLE_NOW	IN	External Sample Command
DATALOG_N	IN	Enable/Disable FIFO
AMX_ENA	OUT	Analog MUX Enable
AMX_SEL(2:0)	OUT	Analog MUX Select Bus
FIFO_FULL	OUT	Indicates that the FIFO is full
REFRESH_DISABLE_N	IN	Enable/Disable EEPROM Refresh
CLOCK_RATE	IN	SYSCLOCK rate (1=1MHz, 0=100Khz)
TESTMODE_N	IN	Manufacturing Test Signal

2.1.1 Functional Block Diagram (Module Level)

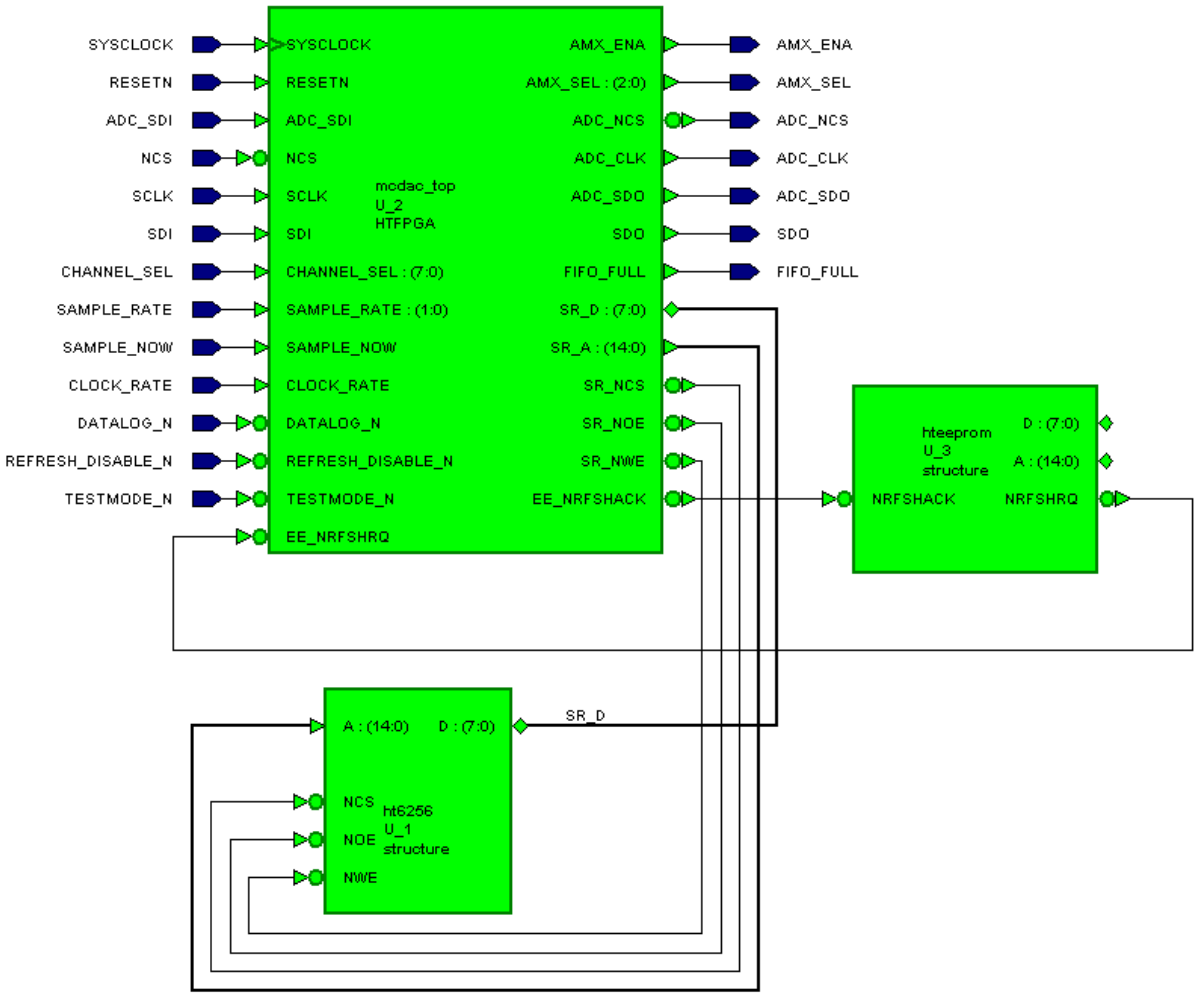


Figure 2 - MCDAC Block Diagram

Figure 2 shows the basic functional block diagram of the MCDAC implemented in the RPDA. This figure shows the representation of the SRAM which is used as the memory portion of a FIFO, and the EEPROM which is only used as the configuration boot memory for the HTFPGA. Note: RPDA connections between HTFPGA and HTEEPROM dedicated to configuration download or test and debug are not shown.

2.1.2 Functional Block Diagram (HTFPGA Configuration Level)

Figure 3 shows the MCDAC design as implemented within the HTFPGA. Primary function and operation are described in the following sections.

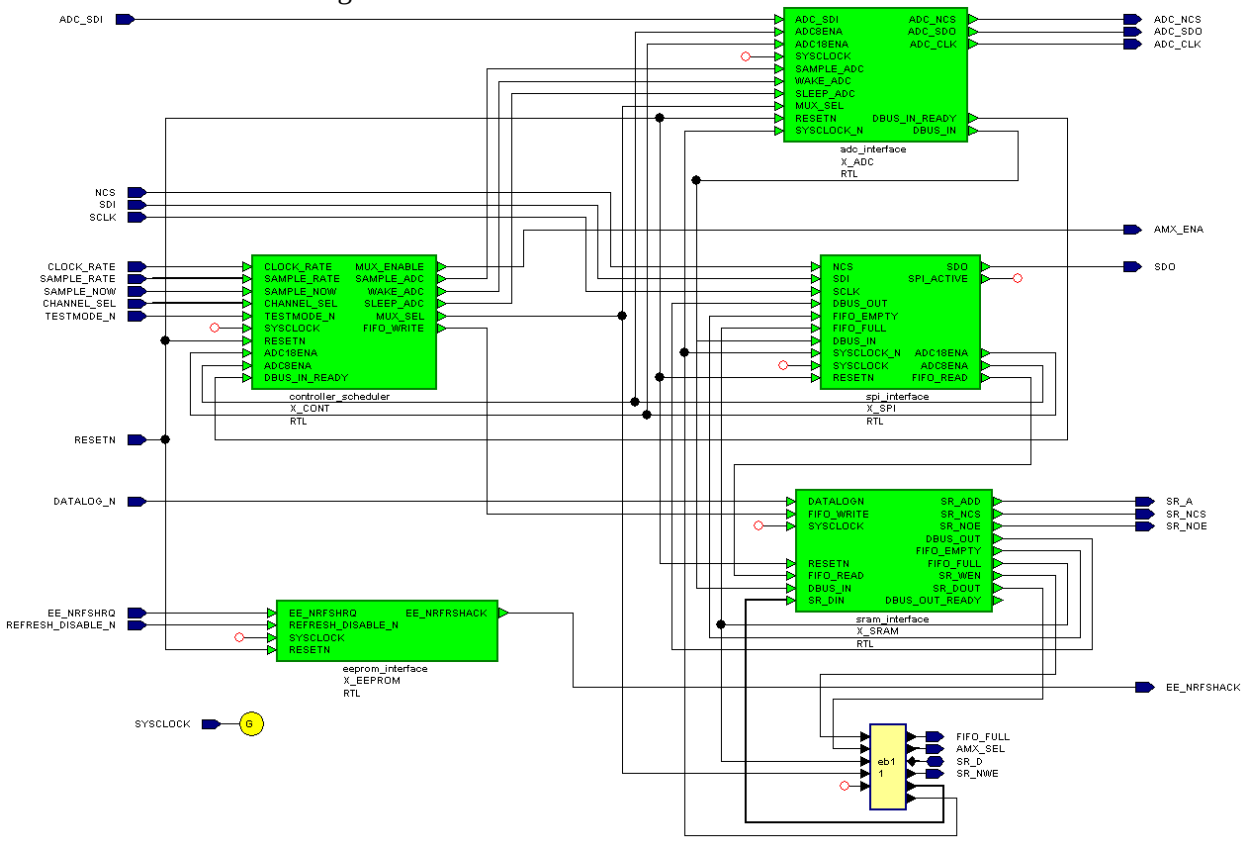


Figure 3 - MCDAC HTFPGA Configuration

2.1.3 Power-on Boot

The primary component in this module is an HTFPGA which has equivalent functionality as ATMEL's AT6010 device [4]. The HTFPGA powers up in an unprogrammed state and must go through a boot up sequence [5]. During this time, internal handshaking between the HTFPGA and the HTEEPROM loads configuration programming into the HTFPGA, programming it into the MCDAC function. In order for this to be accomplished, the user must assure that the HTFPGA mode pins are in their correct state. This is best implemented by hard wiring the M0, M1 and M2 pins to "Mode5" using VDD and VSS (see Table 3).

Table 2 - HTFPGA BOOT MODE CONTROL

Pin	"Mode 5" State	Soft Reboot
M2	1	0
M1	0	0
M0	1	0

Power-on configuration will take up to 300 milliseconds to complete, depending upon conditions (it will take longer at higher temperatures than at lower temperature). During the boot up sequence, all of the HTFPGA configurable IO will be set to a pull-up state. During the boot phase, the HTFPGA/HTEEPROM handshake will perform a self-check function to confirm that the load occurred without error. Should an error be detected, a recheck will occur. If no error in the load is detected on the second check, the ERRN flag will go high and normal functional operation will proceed. If an error is still detected the ERRN flag will remain low and the device will proceed into functional mode, however functional operation may be compromised. Figure 4 shows the general boot sequence.

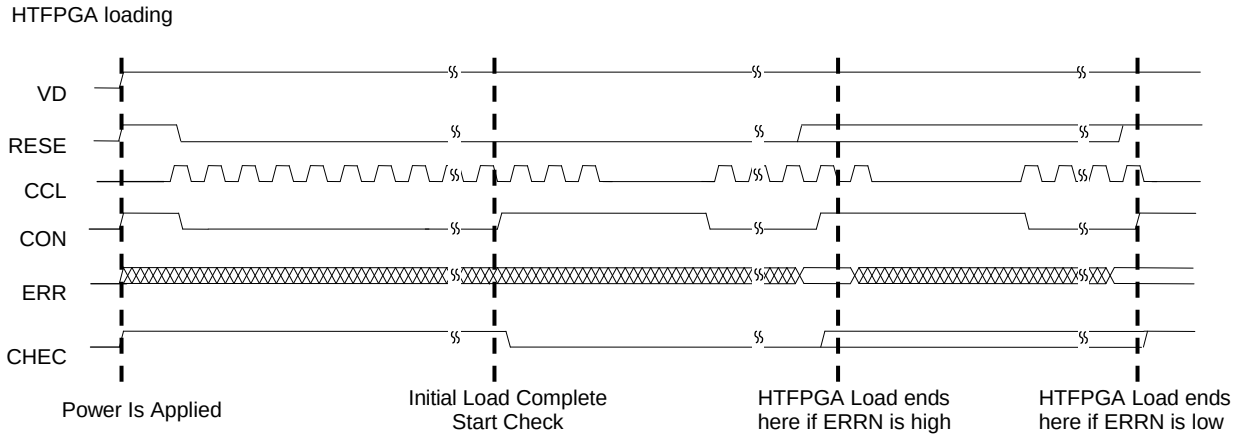


Figure 4 - Boot HTFPGA Load Sequence

Once the configuration is loaded, the internal handshaking will release RESETN and the device will respond to external stimulus and begin functional operations. The module will power up ready to collect data from both the 18-bit and 8-bit converters of the HTADC18. If the SAMPLE_RATE pins are programmed to a non-zero condition, then the unit will begin autonomous operation data collection. If the SAMPLE_RATE bus is set to all zeros, then the unit will collect data when the SAMPLE_NOW pin is toggled. Operational functions are described below.

A soft reboot of the HTFPGA can be forced by driving the M0, M1, M2 pins all to “0” and driving CONN low. This will invoke a reload of the configuration data. See the ATMEL AT6000 series application notes for further information. Most users wishing to re-initiate the module will generally do so by cycling power.

2.1.4 Slave Serial Peripheral Interface (SPI)

The Slave SPI interface allows external communication with the MCDAC, and is the means for collecting data from the module. The MCDAC will operate as a slave on an SPI bus and requires an external SPI Master to initiate data transfers using the SPI port pins.

2.1.4.1 SPI Functional Description:

The Serial Peripheral Interface Slave function provides a means for an external microcontroller operating as an SPI Master to access the results of A-to-D data logged within the MCDAC. Furthermore, the SPI allows some features of the MCDAC to be controlled. These control functions consist primarily of the ability to enable and disable A-to-D operations to reduce power consumption. The SPI port is used to write the internal SPI Control Register and read the HTADC18 data. The status register can be read along with the data or separately. The following are the SPI port signal pins of the MCDAC:

Table 3 - SPI Port Signal Pin Definitions

Pin name	Direction	Description
SCLK	Input	Serial clock
SDI	Input	Control data
SDO	Output	ADC and Status data
NCS	Input	Low asserted chip select

2.1.4.2 SPI Protocol Defined Modes

Microcontrollers available from various vendors implement an SPI port that supports four SPI Modes of operation. The SPI Mode determines how data is exchanged using the clock and data signals of the bus. The SPI Mode is typically selected by properly programming two microcontroller programmable control bits, CPHA and CPOL, which set the SPI Mode. These modes are defined as follows:

The CPOL control bit defines the clock polarity:
0 = Active high clock pulse, low clock when idle
1 = Active low clock pulse, high clock when idle

The CPHA control bit defines the clock phase which determines clock-data relationship for data transfer.
0 = Input data is latched on leading edge of clock pulse. Output data change is triggered by trailing edge of clock pulse.
1= Input data is latched on the trailing edge of the clock pulse. Output data change is triggered by the leading edge of the clock pulse.

These are further defined as SPI mode numbers in the table below:

Table 3 - SPI MODES

Mode Number	CPOL	CPHA	Clock Pulse	Input Data Latched	Output Data Change
0	0	0	Active High	CLK rising edge	CLK falling edge
1	0	1	Active High	CLK falling edge	CLK rising edge
2	1	0	Active Low	CLK falling edge	CLK rising edge
3	1	1	Active Low	CLK rising edge	CLK falling edge

Per section 8.4, 8.5.3 and 8.5.4 of the M68HC11E Family Data Sheet Rev. 5.1, 7/2005.

The MCDAC provides a fixed implementation of the SPI Modes and mode controls and implements the SPI Mode number 3 (CPOL = 1, CPHA =1).

2.1.4.3 SPI Control/Status Register

The SPI Control Register is used to direct the operation of the MCDAC. The SPI Control/Status Register bits are set or cleared depending on the content of the SPI Control Word which is the input bit stream received over SDI, Serial Data In pin (see Table 4).

Table 4 - Control/Status Register Definitions

Bit name	Significance	Configuration Power-on state	Description
Update	Bit 7	Cleared(Low)	When HIGH, the SPI Control register gets updated
Mode(1)	Bit 6	Set (High)	When "10", gets data from FIFO. When "11", gets data most recent ADC data. When "00" or "01", only download status register
Mode(0)	Bit 5	Set (High)	
ADC18ENA	Bit 4	Set (High)	HIGH level enables the 18-bit ADC
ADC8ENA	Bit 3	Set (High)	HIGH level enables the 8-bit ADC
FIFO_FULL	Bit 2	Cleared (Low)	Indicates FIFO is full, no user input
FIFO_EMPTY	Bit 1	Set (High)	Indicates FIFO is empty, no user input
Null	Bit 0	Cleared(Low)	Reserved for future use

2.1.4.4 MCDAC SPI Output Data Formats

The primary function of the MCDAC SPI bus is to permit the retrieval of logged data. Limited control of the external ADC is also possible. To facilitate this, the MCDAC has been provided with the capability of enabling and disabling the 18-bit and 8-bit converters (noted from here on as ADC18 and ADC8). Two SPI output data formats are provided to permit data transfers with the least amount of performance overhead for the cases where: (1) the user wishes to query to FIFO status, but not perform a download (2) the user wishes to access the data that has been stored in the MCDAC. Regardless of the SPI data format selected, it is always possible to read and write the contents of the embedded SPI Control Register over the SPI interface.

The MCDAC SPI data format is set by programming the Mode(1:0) bits in the SPI Control Register as shown in the table below. An 8-bit read/write of the SPI Control Register can be made in any of these formats. The SPI data formats have been implemented so that the 8-bit status word is always read out first to provide for efficient software manipulation.

Table 5 - MCDAC SPI Output Data Format

	Mode(1:0)	Output Format
Status Register Only	"00" or "01"	8 Bits: <Status(7:0)>
Current Data	"11"	40 Bits: <Status(7:0)><SEL(2:0)><ORBit><ADC18(19:0)><ADC8(7:0)>
FIFO data	"10"	40 Bits: <Status(7:0)><SEL(2:0)><ORBit><ADC18(19:0)><ADC8(7:0)>

Key:		
	Status(7:0)	Configuration register bits
	ORBit	over-range bit indicator
	SEL(2:0)	AMUX channel
	ADC18(19:0)	18-bit ADC data
	ADC8(7:0)	8-bit ADC Data

For the 40 bit word, the SEL and ORBit values are stored along with each ADC18 and ADC8 measurement cycle. The SEL indicates which channel was in effect when the ADC measurement occurred. A logic one in ORBit is indicates that the 18-bit ADC modulator input was over-range. See the HTADC18 data sheet [2] for further information on use and operation of this device.

2.1.4.5 SPI Status Read/Control Register Write

An 8-bit SPI Control Register Write with Status Read operation is selected when the MODE(1:0) bits are "00". The SPI Control Register write/Status Register read is initiated by asserting NCS pin LOW. The master must wait for at least four cycles of the SYSCLOCK (nominally 1MHz) before it begins clocking SCLK to begin shifting the data out of the SDO pin. The Status Register word is shifted out serially via the SDO pin, MSB first, with the SDO being updated with serial data at the falling edge of the SCLK. The falling edge of SCLK is used so that SDO data is stable and can be clocked in by the SPI Master at the next rising edge of the SCLK. The SPI Master toggles the SCLK pin LOW-to-HIGH 8 times, then SPI Master terminates the transfer by driving NCS back to HIGH level. Any SCLK clocks over the required 8 will shift zeros out the SDO pin.

When an SPI Write is used to update the SPI Control Register, the SPI Master transmits the SPI Control Word to the MCDAC over the SDI pin. The SPI Master will sequentially shift a new bit of the SPI Control Word out the SDI pin with each falling edge of SCLK beginning with the MSB bit which is shifted out first. The SPI Control Word is then transferred over the SDI and clocked into the internal MCDAC shift register using the rising edge of the SCLK to clock in the data. The SPI Control Word is latched into the SPI Configuration Register when the SPI Master drives the NCS back to HIGH but only if the Update bit of the incoming SPI Control Word is set. Any SCLK clocks over 8 will be ignored for input. If the Update bit is zero, the SPI Control Register will not be updated, though the status will still be shifted out the SDO pin. The SPI write allows the master to write in SPI Control Register concurrently with the SPI read of the previous status. The timing diagram of the MCDAC SPI Control Register write and concurrent SPI Control Register read is shown in Figure 5.

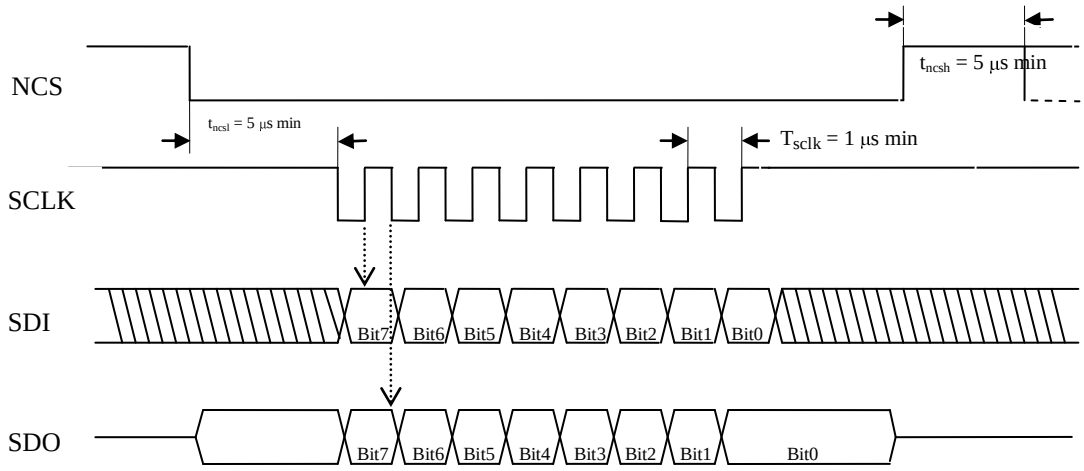


Figure 5 - SPI Control Register Write with Status Read

2.1.4.6 SPI ADC Data Reads (40-bit)

An SPI read of the ADC (FIFO or Most Recent) data can be initiated at any time. An SPI read of the ADC data is initiated by the master driving the NCS pin LOW (while still maintaining SCLK HIGH). The master must wait for at least four cycles of the SYSCLOCK (nominally 1MHz) before it begins clocking SCLK to begin shifting the data out of the SDO pin. While SPI can operate with up to the maximum specified SCLK frequency, the SPI Master must guarantee that the 8th SCLK clock cycle occurs no earlier than 12 cycles of the SYSCLOCK after the falling edge of NCS.

The MCDAC's ADC data will be shifted out the SDO pin on the falling edge of the SCLK. The output shift register driving the SDO pin is clocked out at each falling edge of the SCLK so that the corresponding data bit can be captured by the SPI Master on the next rising edge of SCLK. The 8-bit Status copy of the SPI Control Register is shifted out the SDO pin first, beginning with the MSB, and continues shifting until the LSB of the SPI Control Register data has been output. The MCDAC ADC data samples are then sent - MSB first – and output sequentially until all data bits have been shifted out the SDO pin. The SPI Master then drives SCLK HIGH followed by NCS HIGH to complete the data transfer. The SPI Master must wait for at least one cycle of the SYSCLOCK before initiating a new SPI cycle by driving NCS low.

The 8-bit SPI Control Register can also be written during the ADC Data Read transfers. To accomplish this, the SPI Master drives data to be clocked into the SPI Control Register over the SDI concurrent with the read of the ADC serial data. The SPI Master transitions the SDI data on each falling edge of the SCLK so that it will be stable for clocking into the MCDAC at the next rising edge of the SCLK. The SDI data is shifted in MSB first and loaded into an internal shift register. The SPI Control Register is updated with the shifted in Control Word when the SPI Master drives the NCS HIGH. Only the first 8 bits of SPI data are clocked into the SPI Control Register. Extraneous SDI pin input data that is associated with the additional SCLK transitions of the data 40-bit read are ignored.

A timing diagram illustrating the ADC data read and concurrent SPI Control Register write is shown in Figure 6.

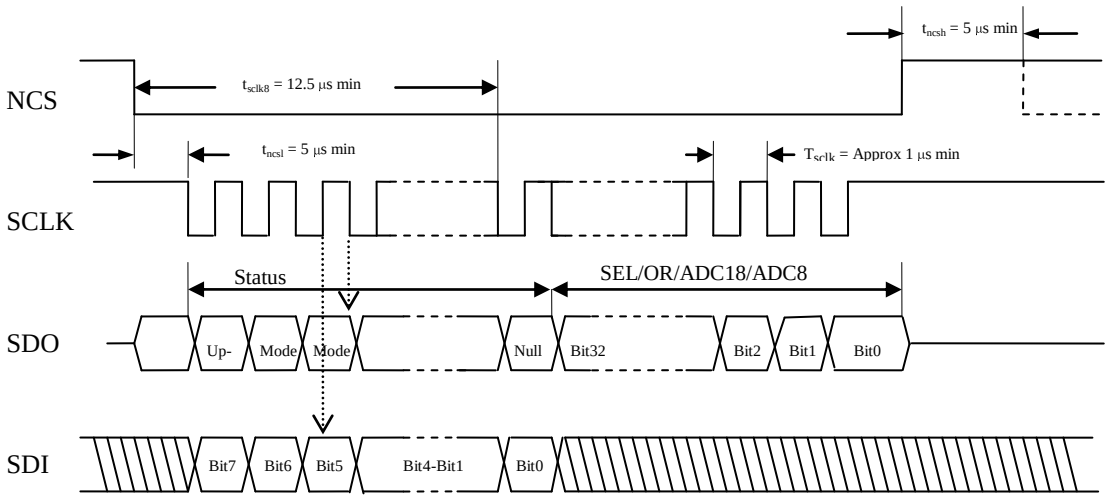


Figure 6- SPI Control Register Write with Data Read (40Bit)

2.1.5 ADC Interface

The MCDAC module has a four-port interface ADC SPI master that will connect directly to the SPI slave pins of the HTADC18. This interface will operate synchronously at SYSCLOCK rates. The ADC_CLK, ADC_NCS, ADC_SDI and ADC_SDO port should be connected to the HTADC18 SCLK, NCS, SDO and SDI pins respectively (see Figure 7).

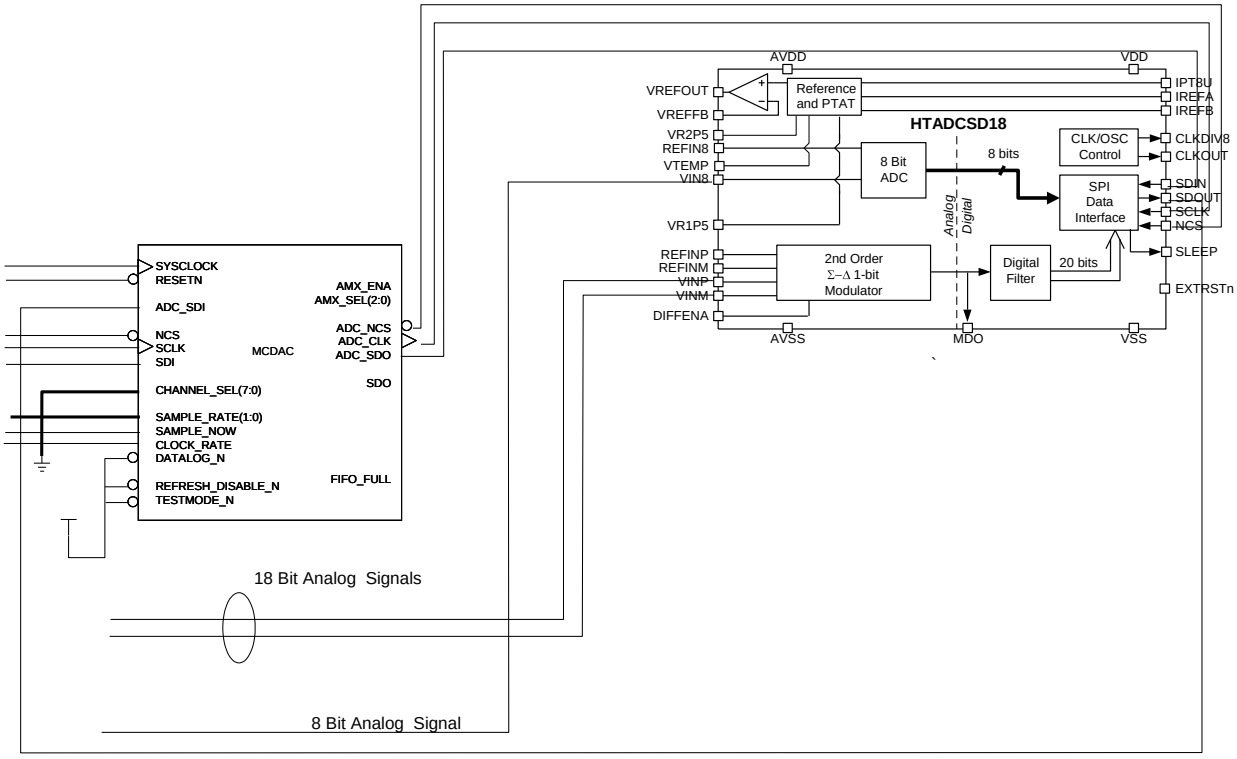


Figure 7 - MCDAC / HTADC18 Connection Diagram

2.1.6 Data Sampling Schedule

The HTADC18 uses a sigma-delta converter for the high-precision 18-bit ADC function. Per the application notes [2], the 18-bit converter requires 0.68 seconds to settle after a step function response. Because the module is intended for use in operations that switch analog inputs into the HTADC18, this step response time establishes a relatively long timing factor in the data acquisition schedule.

The MCDAC control section operates on an internally derived timer that is based on the 1MHz SYSCLOCK. The controller will step through a predefined sequence of events in which the HTADC18 is sent a wake command, data is allowed to settle, both 18-bit and 8-bit data is transferred from the HTADC18 and stored in the FIFO, and the HTADC18 is sent a sleep command. This operates on a 1-second cycle (actually SYSCLOCK_period*1E6). During the sleep period, the analog MUX channels are advanced. Once the sequence is initiated, all of the channels that are active (based on CHANNEL_SEL(7:0)) will be sampled, which can take up to 8 seconds to perform one complete datalog sequence.

Note that although the 8-bit data converter has a high bandwidth and is not limited to a minimum 0.68 second response to a step function, it will be sampled simultaneously as the 18-bit, and so will be on the same 1-second sample cycle.

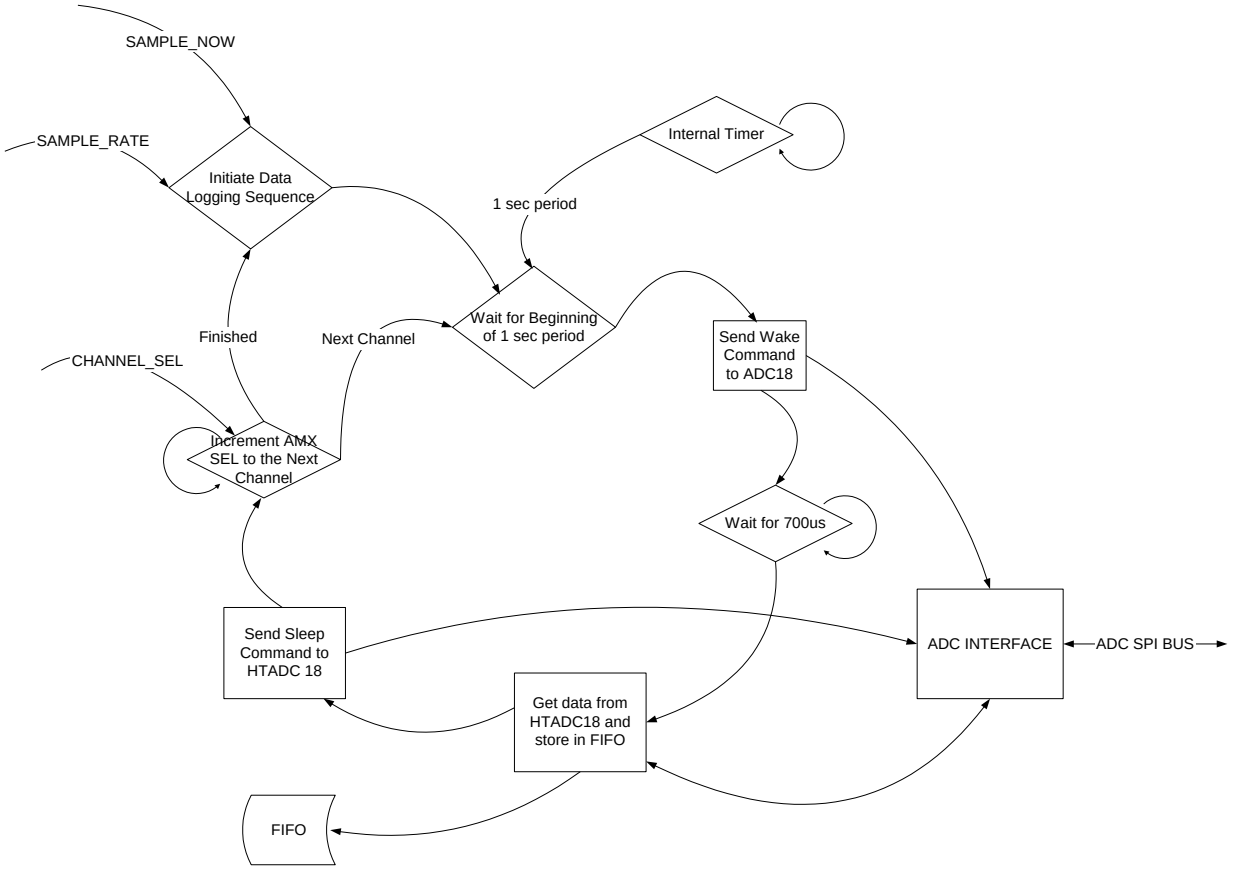


Figure 8 - State Diagram of Data Logging Function

2.1.7 Analog Data Channel Selection

The MCDAC can be programmed to direct the Analog MUX to select any combination of 1 to 8 channels. This is accomplished by setting the CHANNEL_SEL(7:0) masking pins to the appropriate states. Each bit of the CHANNEL_SEL bus corresponds to the same channel of the AMUX. Setting a particular bit to "1" will cause the MCDAC to activate that analog channel and log the data for that channel at the scheduled time. Setting the bit to "0" will cause the MCDAC to skip over that channel when performing the measurement and logging operation.

Note: if the CHANNEL_SEL(7:0) is set to "00000000", the behavior will be the same as setting it to "00000001" that is, it will not disable data measurement but will only activate and measure the first analog channel. This is intended for applications that do not need multi-channel data recording, and so can leave the AMUX out of the system.

2.1.8 Autonomous Operation

One mode of operation for the MCDAC is autonomous operation. In this mode, the internal scheduler will perform the measurement and logging sequence automatically. The period of measurement is based on the settings of the SAMPLE_RATE(1:0) bus which is used to program an internal timer. The timing of the sampling interval is derived from the following equation:

Sample_Period =

SYSCLOCK_period * 1E6 * [60 ^ [SAMPLE_RATE(1)*2 +SAMPLE_RATE(0)*1]] / (10 ^ CLOCK_RATE)

Setting CLOCK_RATE to "0" allows the use of a 100KHz SYSCLOCK while still maintaining an internal 1 second timebase. If the SAMPLE_RATE="01", then the sample period may be shorter than the time required to sequence through each of the channels, therefore the sample rate for each channel will be the number of channels.

If the SAMPLE_RATE(1:0) is set to "00", the behavior will default to Sample-On-Demand (see 2.1.9).

SAMPLE_RATE Example:
For a 1MHz SYSCLOCK, the autonomous sample period for the MCDAC is as shown in Table 6.

Table 6 - SAMPLE_RATE Selection Example for 1MHz Clock (CLOCK_RATE=1)

SAMPLE_RATE(1:0) Selection	SYSCLOCKs Between Samples (1E6 clocks)	Nominal Period (HH:MM:SS)
00	NA	Sample-on-demand
01	1	00:00:01
10	60	00:01:00
11	3600	01:00:00

2.1.9 Sample-on-Demand

The second mode of operation for the MCDAC is Sample-on-Demand. When the SAMPLE_RATE is programmed to "00", the SAMPLE_NOW input becomes enabled. In this mode, the SAMPLE_NOW value is latched into the scheduler on rising SYSCLOCK. The scheduler maintains an internal 1 second period. At the beginning of each period, the scheduler checks for the latched SAMPLE_NOW. If the signal was detected, then the device will initiate a measure and logging sequence, sampling each of the channels as determined by the CHANNEL_SEL programming on the normal 1 sec interval. After all channels have been sampled, the module will return to a wait state, until the next time SAMPLE_NOW is toggled.

SAMPLE_NOW is latched into the module with SYSCLOCK, therefore it is necessary that the SAMPLE_NOW signal be held high a minimum of two SYSCLOCK periods in order to guarantee detection of the sample request.

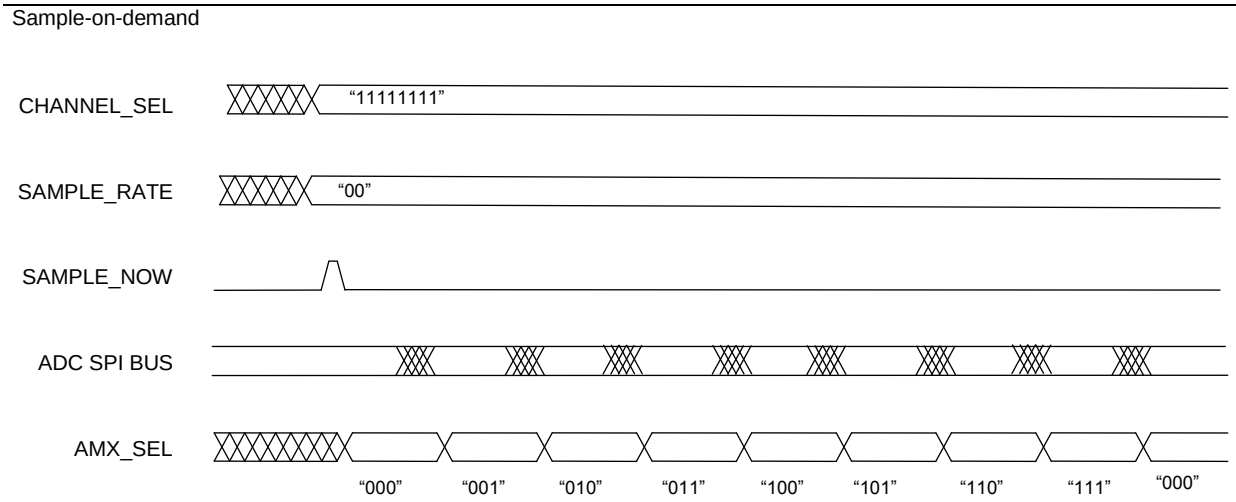


Figure 9- Data Sample Sequence

2.1.10 FIFO DATALOG_N Disable

A means of manually disabling data logging in the FIFO is provided with the DATALOG_N pin. When low, all measurements are stored in the FIFO. If the DATALOG_N is held high, then the FIFO will be disabled from writing data. The measurements will still be made, and will be available to the SPI bus for downloading (in "Recent Data" mode). This function is intended for operations in which data logging may not be desired, such as equipment insertion or extraction, or when an external set point determines that data should be logged.

2.1.11 HTEEPROM Refresh Disable

The HTEEPROM within the MCDAC implements a refresh strategy to provide reliable data retention for 5 years. Refresh circuitry will rewrite all bits in the EEPROM at power-on and then approximately once per month. An interrupt style handshake is implemented in this design so that the MCDAC is not affected by the refresh function.

The duration of the refresh process will be approximately 5 seconds. This occurs immediately upon powering up the module and after configuration of the HTFPGA has occurred. Any application that uses this component must provide power to the device for a minimum of 5 seconds to allow for the HTEEPROM function to complete. The REFRESH_DISABLE_N pin is provided for users who wish to disable the refresh function. The user must however provide some means of allowing refresh to occur regularly or risk losing the functionality of the module.

Users of this product should be aware that the HTEEPROM has a limited number of refresh cycles that can be allowed during the lifetime of the product. Applications that will undergo a large number of power cycles may exceed the write cycle limit and affect the reliability of the boot-configuration operation. These applications should take advantage of the REFRESH_DISABLE_N function wherever possible, keeping in mind the need to perform a refresh at least once every 40 days. The total allowable power+refresh cycles before impacting reliability is TBD.

3 Detail Specifications

3.1 IO Descriptions

The following table is a listing of all the signals and their purpose. Package pin mapping is shown in Table 10.

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
A12 B13 B12	M0 M1 M2	D	I	-	Mode Control For HTFPGA. User should select Mode 5 (M0=M2=VDD,M1=VSS)
A13	SYSCLOCK	D	I	-	1MHz System Clock
A14	RESETN	D	IO	-	Master Reset – Active Low
F9	CLOCK_RATE	D	I	-	Indicates to MCDAC that SYSCLOCK is either 1MHz (high) or 100KHz(low)
A6	SDI	D	I	-	Slave SPI bus controller
A5	NCS	D	I	-	Slave SPI bus controller
A8	SCLK	D	I	-	Slave SPI bus controller
A7	SDO	D	O	-	Slave SPI bus controller
A11	ADC_CLK	D	O	-	ADC Master SPI bus controller
B11	ADC_NCS	D	O	-	ADC Master SPI bus controller
A10	ADC_SDI	D	I	-	ADC Master SPI bus controller
B14	ADC_SDO	D	O	-	ADC Master SPI bus controller
B10	DATALOG_N	D	I	-	Enable Control for FIFO – Active Low
B6	FIFO_FULL	D	O	-	Indicates that the internal 8Kx32 FIFO has been filled.
G10 G9	SAMPLE_RATE1 SAMPLE_RATE0	D	I	-	Sets the autonomous sample rate. All zeros will only sample on “SAMPLE_NOW” input.
G11	SAMPLE_NOW	D	I	-	External initiation of ADC sampling. Pin is disabled when SAMPLE_RATE(1:0) is not “00”.
F8 F6 G8 G7 F5	CHANNEL_SEL7 CHANNEL_SEL6 CHANNEL_SEL5 CHANNEL_SEL4 CHANNEL_SEL3	D	I	-	Controls which of the eight analog channels is recorded.

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
G6 G5 F7	CHANNEL_SEL2 CHANNEL_SEL1 CHANNEL_SEL0				
A9	AMUX_ENA	D	O	-	Analog MUX Enable Control
B9 B8 B7	AMUX_SEL2 AMUX_SEL1 AMUX_SEL0	D	O	-	Analog MUX Select control
F10	TESTMODE_N	D	I	-	Test function. Accelerates the autonomous sample rate by 100X
F11	REFRESH_DISABLE_N	D	I	-	Disables EEPROM refresh function.
The following RPDA pins are not intended for use by the end user, and should be biased or left unconnected as indicated					
G12	UNRSTN	D	I	PU	Reboot Bypass Function. User should leave open or tie high.
C1 C2 D1 B3 B4 C3 B2 E1 F1 D2 F2 E2 G4 G3 F4	SR_A14 SR_A13 SR_A12 SR_A11 SR_A10 SR_A9 SR_A8 SR_A7 SR_A6 SR_A5 SR_A4 SR_A3 SR_A2 SR_A1 SR_A0	D	O	-	Monitor of SRAM Address. – Leave unconnected
B5 B4 C5 D3 D4	SR_D7 SR_D6 SR_D5 SR_D4 SR_D3	D	O	-	Monitor of SRAM Data – Leave Unconnected

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
E3 E4 F3	SR_D2 SR_D1 SR_D0				
A4	SR_NCS	D	O	-	Monitor of SRAM NCS - Leave unconnected.
A3	SR_NOE	D	O	-	Monitor of SRAM NOE - Leave unconnected.
B1	SR_NWE	D	O	-	Monitor of SRAM NWE - Leave unconnected.
C19 B20 C18 B19 C17 B18 E19 C16 B17 A18 C15 B16 A17 B15 D14	EE_A14 EE_A13 EE_A12 EE_A11 EE_A10 EE_A9 EE_A8 EE_A7 EE_A6 EE_A5 EE_A4 EE_A3 EE_A2 EE_A1 EE_A0	D	O	-	Monitor of EEPROM Address - Leave unconnected.
D21 C20 E20 E19 E18 E17 E16 E15	EE_D7 EE_D6 EE_D5 EE_D4 EE_D3 EE_D2 EE_D1 EE_D0	D	O	-	Monitor of EEPROM Data I/0 - Leave unconnected.
E14	EE_CSN	D	O	-	Monitor of EEPROM Chip Select - Leave unconnected.
G13	EE_OEN	D	O	-	Monitor of EEPROM Output Enable - Leave unconnected.
F14	EE_WEN	D	O	-	Monitor of EEPROM Write Enable - Leave unconnected
F13	EE_CFG_PROT	D	I	-	EEPROM - Configuration Protection – Tie to VDD
F15	EE_SELSNP	D	I	PD	EEPROM Product Interface Mode: Select Serial NOT Parallel: - Tie to VSS
G18	EE_SO	D	O	-	EEPROM Serial Data Output - Leave

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
					unconnected.
F16	EE_SI	D	I	PU	EEPROM Serial Data Input - Leave unconnected.
G15	EE_SCK	D	I	PU	EEPROM Serial Clock - Leave unconnected.
G16	EE_WPN	D	I	PU	EEPROM - Write Protect - Leave unconnected.
F17	EE_HOLDN	D	I	PU	EEPROM Hold/Pause of serial transmission - Leave unconnected.
G17	EE_SBP0	D	I	PU	EEPROM Serial Mode Block Protect Bit 0 - Leave unconnected.
F18	EE_SBP1	D	I	PU	EEPROM Serial Mode Block Protect Bit 1 - Leave unconnected.
G19	CCLK	D	IO	PU	HTFPGA Configuration Clock - Leave unconnected.
G14	ERRN	D	IO	PU	HTFPGA Data Validation Error - Leave unconnected.
F19	CHECKN	D	IO	PU	HTFPGA Data Validation Signal - Leave unconnected.
F20	CONN	D	IO	PU	HTFPGA Configuration Control - Leave unconnected.
A15	EE_NRFSHRQ	D	O	-	Monitor of EEPROM Data Refresh - Leave unconnected.
A16	EE_NRFSHACK	D	O	PU	Monitor of Refresh Acknowledgement - Leave unconnected.
A21	POROUTN (EEPROM PORINN)	D	IO	PU	Monitor of Power-on-Reset Activity - Leave unconnected.
D19	TM_VP	HVP	IO	-	EEPROM Positive High Voltage Supply - Leave unconnected.
D17	TM_VM	HVM	IO	-	EEPROM Negative High Voltage Supply - Leave unconnected.
D18	TM_NSELHALF	D	I	PU	EEPROM Select Half of All Rows Test Mode – Leave unconnected
D15	TM_NRFSHOSC and TM_ECC_NDISABLE	D	I	PU	Connected simultaneously to both EEPROM - Refresh Oscillator Test pin and EEPROM ECC Disable Test pin- Leave unconnected.
D16	TM_NRFSHDIV and TM_NPOE	D	I	PU	Connected simultaneously to both EEPROM Refresh 30 Day Counter Test pin and EEPROM Parallel Outputs Enable Test pin – Leave unconnected.
D20	TMPDIODE	AG	I	-	EEPROM On-Die Temperature Diode - Leave unconnected.
A20	VSSA	AG	-	-	Analog Circuit Ground, user is to tie this to the

Table 7 - MCDAC Pin Description

Module Pin Number	Name	Type	Dir	PU/ PD	Description
					same plane as VSS(1)
A21	VDDA	AS	-	-	Analog 5V Supply, user is to tie this to the same plane as VDD(1)
A2,G2, G20	VSS	G	-	-	Digital Circuit Ground(1)
A1,G1, G21	VDD	S	-	-	Digital 5V Supply(1)
C21, D21, E21	Heater	CT	-	-	Connection to embedded heater. Used during characterization test to heat the package for extended high-temperature test.

(1) All power and ground connections should be made by low-impedance/low-inductance traces on the circuit board.

This key can be helpful in understanding some of the additional details:

Type:

D	Digital (0 = VSS, 1 = VDD) [bipad_dig]
A	Analog (varies between VSS and VDD)
HVP	High Voltage Analog, Positive (0 V to +14 V rel. to VSS)
HVM	High Voltage Analog, Minus (-14 V to 0 V rel. to VSS)
AG	Analog Circuit Ground, 0V, VSSA
AS	Analog Supply, 5 V (typ.), VDDA
G	Digital Ground, 0 V, VSS
S	Digital Supply, 5 V (typ.), VDD
CT	Characterization Test Input

Direction (Dir):

I	Input
O	Output
IO	Bidirectional, Input/Output

Pull Up and Pull Down (PU/PD):

-	None
PU	Pull Up, with type, active/resistive/current
PD	Pull Down, with type, active/resistive/current

3.2 Absolute Maximum Ratings

Table 4 – MCDAC Absolute Maximum Specifications

		Ratings(1)		
Symbol	**Parameter**	**Min**	**Max**	**Units**
VDD	Positive Supply Voltage (2)	-0.5	6.5	Volts
VPIN	Voltage on Any Pin (2, 5)	-0.5	VDD + 0.5	Volts
IOUT	Average Output Current	-20	20	mA
TSTORE	Storage Temperature	-65	250	°C
TSOLDER	Soldering Temperature (5 seconds)		355	°C
PD	Package Power Dissipation (3)		3	W
ØJC	Package Thermal Resistance 147 PGA MCM (Junction to Case)		7.0	°C/W
VPROT	Electrostatic Discharge Protection Voltage (4)	2000		V
TJ	Junction Temperature		300	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.

(2) Voltage referenced to VSS

(3) MCDAC power dissipation due to IDDS, IDDOP, and IDDSEI, plus MCDAC output driver power dissipation due to external loading must not exceed this specification

(4) Class 2 electrostatic discharge (ESD) input protection voltage per MIL-STD-883, Method 3015. This is goal. ESD withstand capability has not been established for all of the components (as of Jan. 31, 2007).

(5) TM_VP and TM_VM test pins are exceptions when data is being written to the HTEEPROM. These pins are connected to the HTEEPROM internal charge-pumps and will typically be at +8.5V (VP) and -8.5V (VSS) during HTEEPROM write operations. Otherwise, during normal operation they are constrained to the voltages in the above table.

3.3 Recommended Operating Conditions

Table 5 - MCDAC Recommended Operating Conditions

			Limits		
Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Units**
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts
VPIN	Voltage On Any Pin (1)	-0.3		VDD+0.3	Volts
CLOAD	Capacitive Output Load			100	pF
TC	Case Operating Temperature	-55		225	°C
TJ	Maximum Junction Temperature			250	°C

(1) Heater input, and VP and VM test pins are exceptions, which are not for use by the user and should be left unconnected.

3.4 DC Specifications

Table 8 - DC Specifications

Symbol	PARAMETER	CONDITIONS[1]	MIN	TYP	MAX	UNITS
VDD	Digital Supply Operational Voltage		4.75	5.00	5.25	V
VDDA	Analog Supply Operational Voltage		4.75	5.00	5.25	V
IDDA	Digital Supply Operational Current	SYSCLOCK=1MHz			100	μA
IDD	Analog Supply Operational Current	SYSCLOCK=1MHz			25	mA
$IDDA_{STDBY}$	Digital Supply Standby Current	Sleep Mode, SYSCLOCK=0Hz			10	μA
IDD_{STDBY}	Analog Supply Standby Current	Sleep Mode, SYSCLOCK=0Hz			2	mA
VDD_{delta}	Supply Offset (VDDA – VDD) or (VSSA – VSS)		-0.3		0.3	V
V_{IH}	High Level Input Voltage		2.5		VDD + 0.1	V
V_{IL}	Low Level Input Voltage		VSS - 0.1		1	V
I_{IN}	Digital Input Leakage	$0 V \leq V_{IN} \leq VDD$	-2		2	μA
V_{OH}	High Level Output	IO = --5.73 mA	VDD – 0.5			V
V_{OL}	Low Level Output	IO = 5.25 mA			0.5	V
I_{OZ}	High-Z Output Leakage	$0 V \leq VOUT \leq VDD$	-2		2	μA
I_{OZ}	High-Z Output Leakage w/PU	$0 V \leq VOUT \leq VDD$	-600		-60	μA
C_{IN}	Input Capacitance		5	10	25	pF

Note 1 – Unless otherwise stated: 4.75<VDD<5.25, VDDA=VDD, -65C< T_{CASE} <225C, C_{LOAD} = 100pF

3.5 AC Specifications

Table 9 - AC Specifications

Symbol	PARAMETER	CONDITIONS[1]	MIN	TYP	MAX	UNITS
T_{BOOT}	Delay from Power-up to CONN Released				300	ms
F_{CLK1}	SYSCLOCK Frequency		0.1		1	MHz
F_{CLK2}	SPI SCLK Frequency		0.1		1	MHz
T_{SETUP1}	Control[2] to SYSCLOCK rising				250	ns
T_{SETUP2}	SR_D to SYSCLOCK rising				150	ns
T_{SETUP3}	ADC_SDI to SYSCLOCK rising				150	ns
T_{HOLD1}	Control[2] to SYSCLOCK rising		100			ns
T_{HOLD2}	SR_D to SYSCLOCK rising		100			ns
T_{HOLD3}	ADC_SDI to SYSCLOCK rising		100			ns
T_{DC1}	SYSCLOCK Duty Cycle		40		60	%
T_{PROP1}	SYSCLOCK falling to ADC_SDO				150	ns
T_{PROP2}	SYSCLOCK falling to ADC_NCS				150	ns
T_{PROP3}	SYSCLOCK falling to ADC_CLK				150	ns
T_{PROP4}	SYSCLOCK falling to SR_D				150	ns
T_{PROP5}	SYSCLOCK falling to SR_A				150	ns
T_{PROP6}	SYSCLOCK falling to AMX_SEL and AMX_ENA				150	ns
T_{DC2}	SPI SCLK Duty Cycle		40		60	%
T_{RISE1}	SCLK Rise Time				15	ns
T_{FALL1}	SCLK Fall Time				15	ns
T_{HIGH1}	NCS High Time		2			SYSCLOCK periods
T_{LOW2}	NCS Low Time		42			SYSCLOCK periods
T_{SETUP5}	NCS to SCLK Setup Time				150	ns
T_{HOLD5}	NCS to SCLK Hold Time		150			ns
T_{PROP7}	NCS to SDO Active Propagation Delay				150	ns
T_{SETUP6}	SDI to SCLK Setup Time				150	ns
T_{HOLD6}	SDI to SCLK Hold Time		150			ns
T_{PROP8}	SCLK to SDO Propagation Delay				300	ns
T_{RISE2}	SDO Rise Time				TBD	ns
T_{FALL2}	SDO Fall Time				TBD	ns

Table 9 - AC Specifications

Symbol	PARAMETER	CONDITIONS[1]	MIN	TYP	MAX	UNITS
T_{HIGH2}	SAMPLE_NOW High Time		2			SYSCLOCK periods

Note 1 – Unless otherwise stated: 4.75<VDD<5.25, VDDA=VDD, -65C< T_{CASE} <225C, C_{LOAD} = 100pF

Note 2 – Control Signals are CHANNEL_SEL, SAMPLE_RATE, REFRESH_DISABLE_N, CLOCK_RATE

3.6 Signal Map

Table 10 shows the mapping of MCDAC signals to package pins. Signal names are color coded to indicate their general function. Note that power, ground and functional signals are near the top and bottom edge. Test signals pins and those who are to be left unconnected by the user are located more towards the center of the package.

Table 10 - MCDAC Signal Map (Bottom View)

g01	g02	g03	g04	g05	g06	g07	g08	g09	g10	g11	g12	g13	g14	g15	g16	g17	g18	g19	g20	g21
VDD	VSS	SR_A(1)	SR_A(2)	CHANNEL_SEL(1)	CHANNEL_SEL(2)	CHANNEL_SEL(4)	CHANNEL_SEL(5)	SAMPLE_RATE(0)	SAMPLE_RATE(1)	SAMPLE_NOW	UNRSTN	EE_OEN	ERRN	EE_SCK	EE_WPN	EE_SBP0	EE_SO	CCLK	VSS	VDD
f01	f02	f03	f04	f05	f06	f07	f08	f09	f10	f11	f12	f13	f14	f15	f16	f17	f18	f19	f20	f21
SR_A(6)	SR_A(4)	SR_D(0)	SR_A(0)	CHANNEL_SEL(3)	CHANNEL_SEL(6)	CHANNEL_SEL(0)	CHANNEL_SEL(7)	CLOCK RATE	TEST MODE_N)	REFRESH_DISABLE_N	CSOUT	EE_CFG_PROT	EE_WEN	EE_SELSNP	EE_SI	EE_HOLDN	EE_SBP1	CHECKN	CONN	POROUTN
e01	e02	e03	e04	e05	e06	e07	e08	e09	e10	e11	e12	e13	e14	e15	e16	e17	e18	e19	e20	e21
SR_A(7)	SR_A(3)	SR_D(2)	SR_D(1)										EE_CSN	EE_D(0)	EE_D(1)	EE_D(2)	EE_D(3)	EE_D(4)	EE_D(5)	Heater
d01	d02	d03	d04	d05	d06	d07	d08	d09	d10	d11	d12	d13	d14	d15	d16	d17	d18	d19	d20	d21
SR_A(12)	SR_A(5)	SR_D(4)	SR_D(3)										EE_A(0)	TM_NRFSHOSCECCNDISABLE	TM NPOE NRFSHDIV	TM_VM	TM_NSELHLF	TM_VP	TMP DIODE	Heater
c01	c02	c03	c04	c05	c06	c07	c08	c09	c10	c11	c12	c13	c14	c15	c16	c17	c18	c19	c20	c21
SR_A(14)	SR_A(13)	SR_A(9)	SR_D(6)	SR_D(5)										EE_A(4)	EE_A(7)	EE_A(10)	EE_A(12)	EE_A(14)	EE_D(6)	Heater
b01	b02	b03	b04	b05	b06	b07	b08	b09	b10	b11	b12	b13	b14	b15	b16	b17	b18	b19	b20	b21
SR_NWE	SR_A(8)	SR_A(11)	SR_A(10)	SR_D(7)	FIFO_FULL	AMX_SEL(0)	AMX_SEL(1)	AMX_SEL(2)	DATALOG_N	ADC_NCS	M2	M1	ADC_SD0	EE_A(1)	EE_A(3)	EE_A(6)	EE_A(9)	EE_A(11)	EE_A(13)	EE_D(7)
a01	a02	a03	a04	a05	a06	a07	a08	a09	a10	a11	a12	a13	a14	a15	a16	a17	a18	a19	a20	a21
VDD	VSS	SR_NOE	SR_NCS	NCS	SDI	SDO	SCLK	AMX_ENA	ADC_SDI	ADC_CLK	M0	SYS CLOCK	RESETN	EE_NRFSHRQ	EE_NRFSHACK	EE_A(2)	EE_A(5)	EE_A(8)	VSSA	VDDA

KEY

- Power
- Ground
- SRAM/FPGA Dual Use
- FPGA Configurable IO
- FPGA Control Signals
- EEPROM/FPGA Dual Use
- EEPROM Only
- Heater Input

3.7 Package Outline

Figure 10 shows the package outline for the MCDAC module. Note that the height dimension does not include the lid, which adds another 0.020 to the over all height.

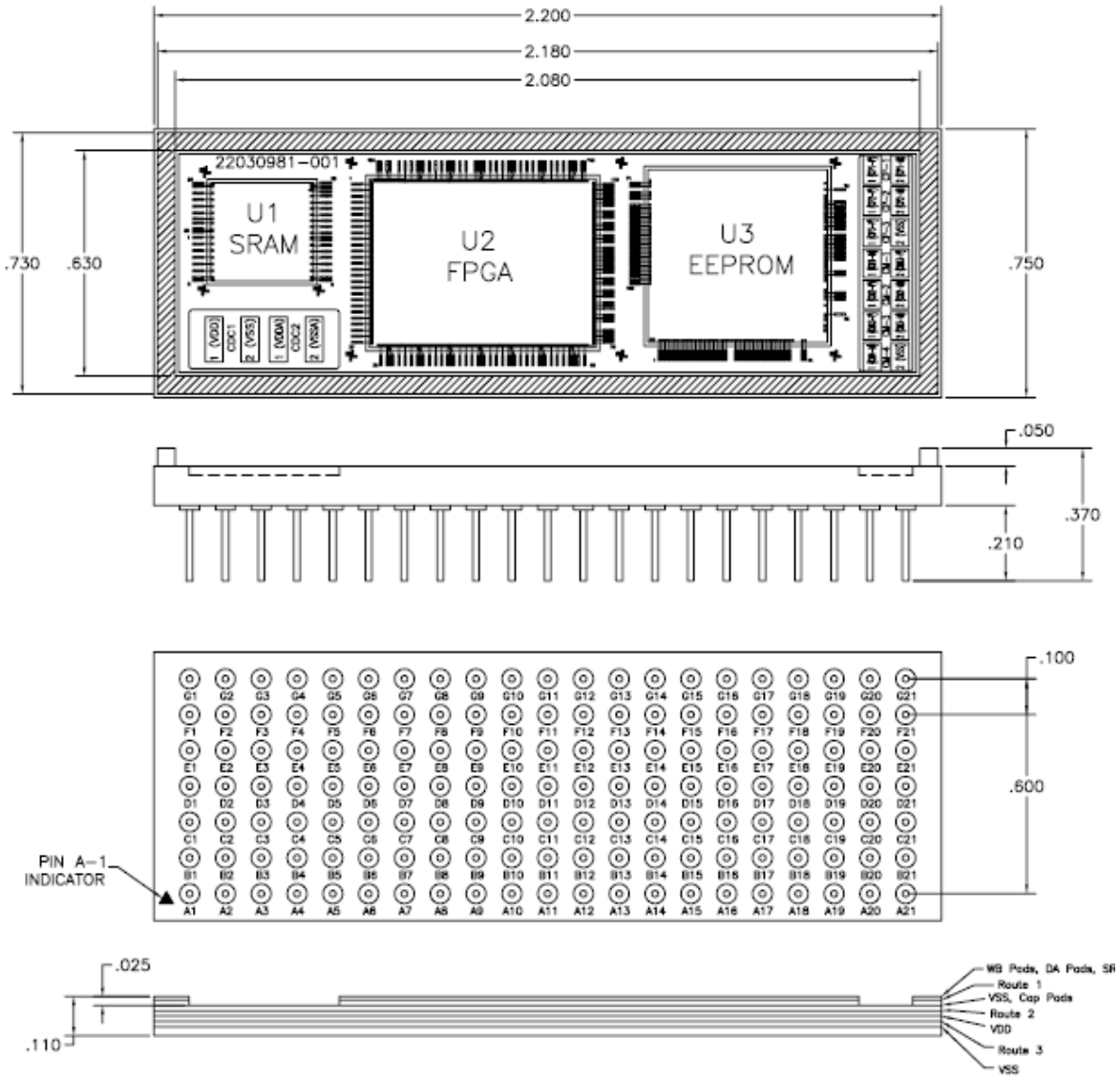


Figure 10 - MCDAC Package Outline

4 Applications

The following diagram illustrates possible modes of operation for the MCDAC.

4.1 Single Channel Operation

For applications that have limited requirements, the MCDAC can be set up in a single channel mode. Tying the CHANNEL_SEL bus to VSS will signal the unit that only one channel of data is to be recorded. If the SAMPLE_RATE is set to "01", then the unit will log data every 1 second (at 1MHz nominal SYSCLOCK). The VIN8 pin of the HTADC18 can be tied to the VTEMP output, should one wish to monitor the on-board temperature probe of the HTADC18. See the HTADC18 datasheet for further information.

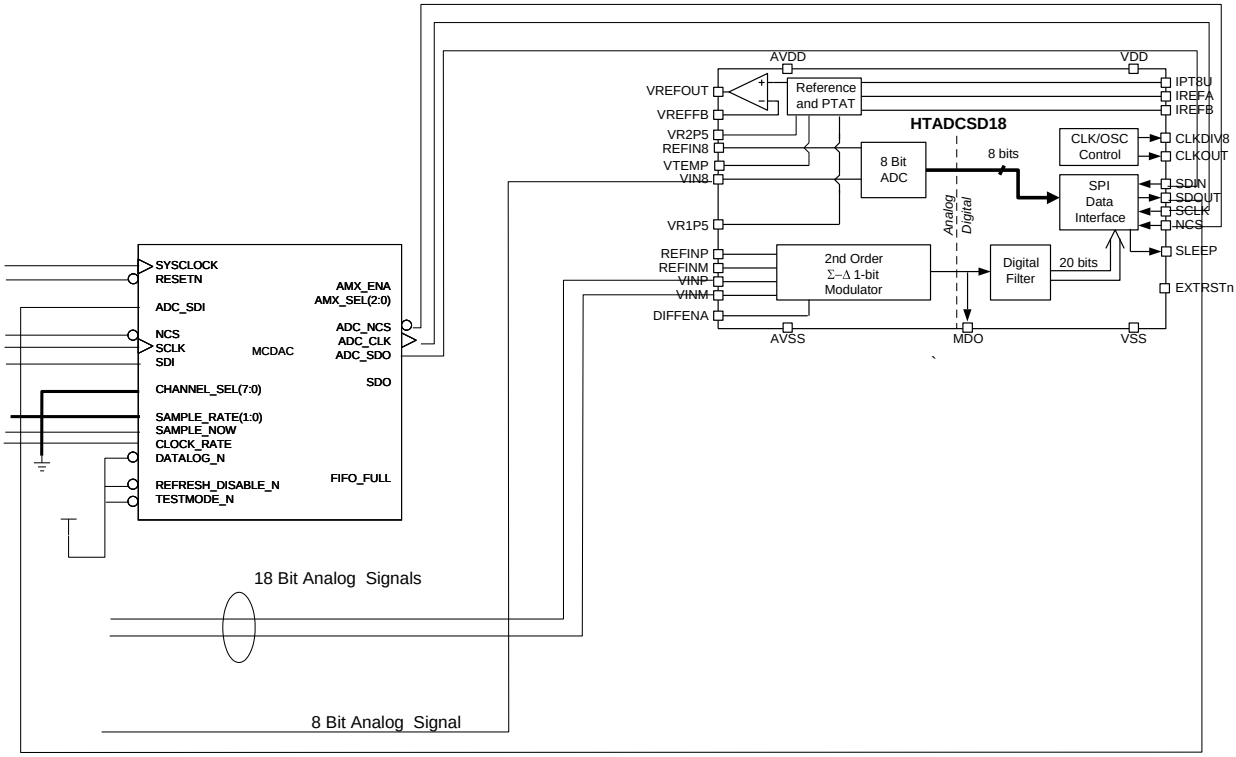


Figure 11- Single Channel Operation

4.2 Multi-Channel 18-bit Operation

For applications that require logging more channels, the MCDAC can be set up in multichannel channel mode, using an HT507 to steer differential analog inputs to the HTADC18 front end. As previously described, setting the CHANNEL_SEL and SAMPLE_RATE signals to the appropriate settings will allow multiple choices in operation.

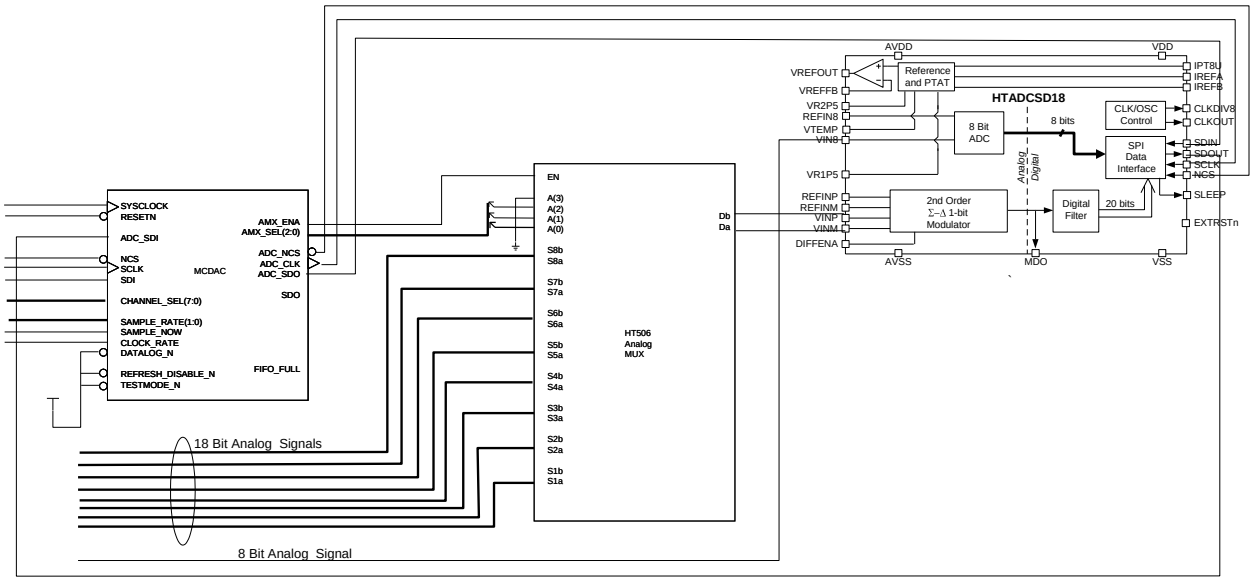


Figure 12 - Multi-channel 18-bit, Single-channel 8-bit Configuration

4.3 Multi-Channel 8-bit and 18-bit Operation

Up to two HT507 devices can be connected in parallel to the AMX pins, should an application wish to datalog multiple 8-bit data along with the 18-bit data.

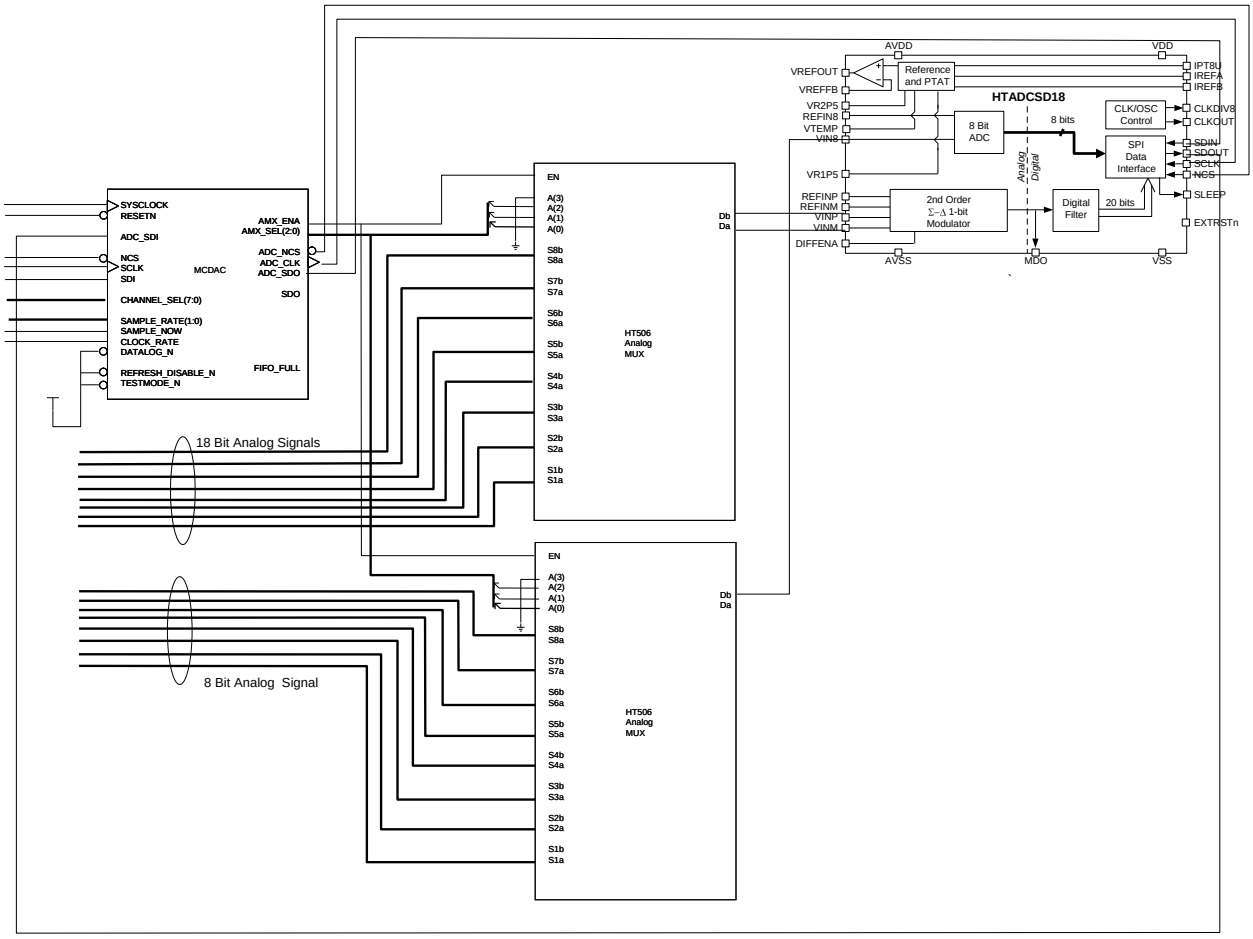


Figure 13 - Multi-channel 18-bit and 8-bit Configuration

5 References

1. Honeywell "*Reconfigurable Processor for Data Acquisition (RPDA) Data Acquisition System Objectives Specification*" Rev 1.0, dated 21 January 2007.
2. Honeywell "*HTADC18 High Temperature 18-bit Differential Input ΣΔ ADC with Built-in Clock, Voltage Reference and SPI Interface*" Datasheet dated 9-15-2006
3. Honeywell *"HT506/507 High Temperature Analog Multiplexers 16-Channel Single / 8-Channel Dual*" Datasheet – 4/98.
4. Atmel *"Coprocessor Field Programmable Gate Arrays AT6000(LV) Series"* dated 10/99
5. Atmel *"Field Programmable Gate Array Configuration Guide"* for AT6000 Series Devices, dated 9/99

High Temperature EEPROM (HTEEPROM) Pad/Signal Definitions

APPENDIX to Final Report

Deep Trek Re-configurable Processor for Data Acquisition (RPDA)

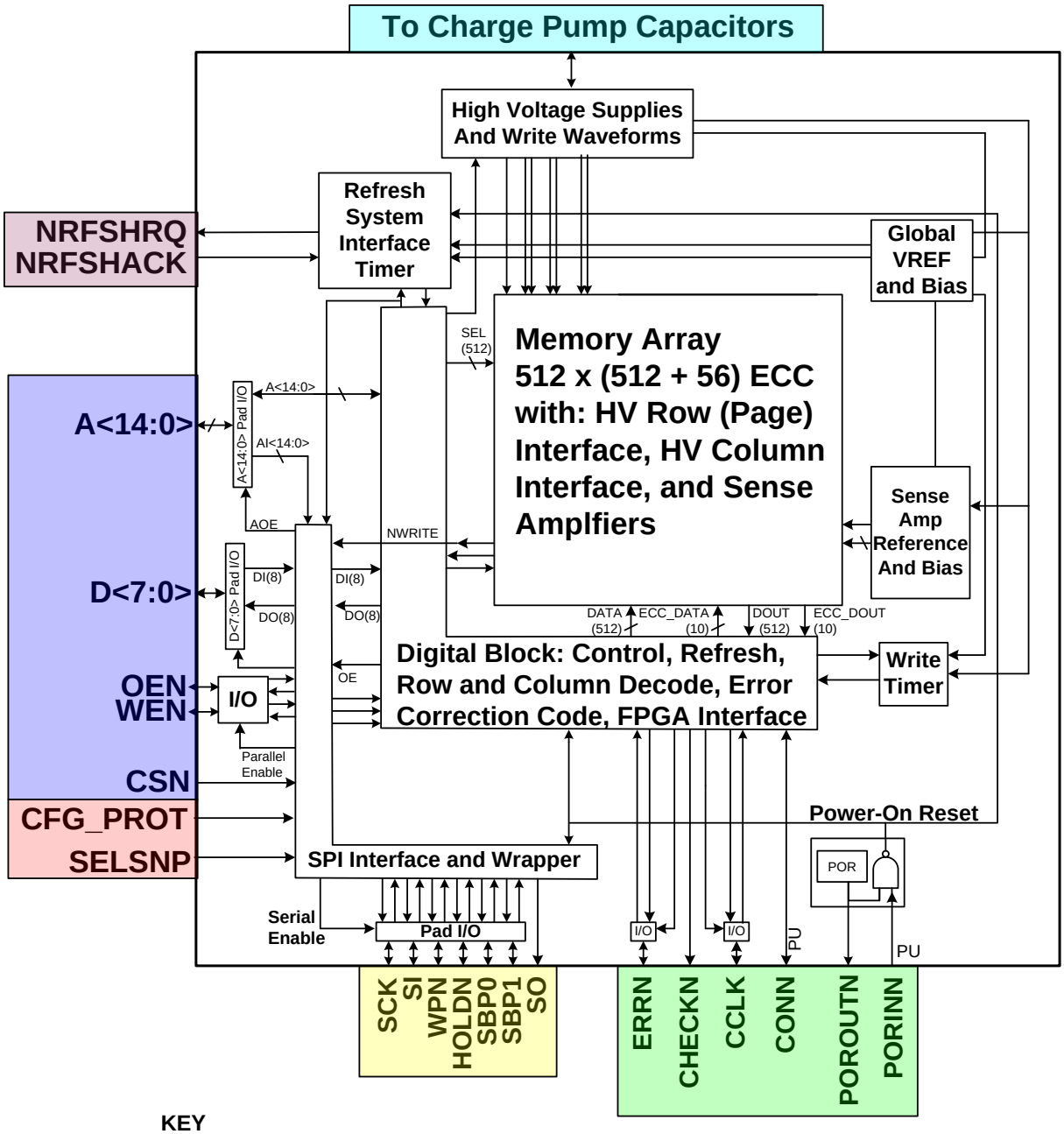
Revision 1.0
24 September 2009

Author:
Bruce Ohme

Honeywell

CONTENTS

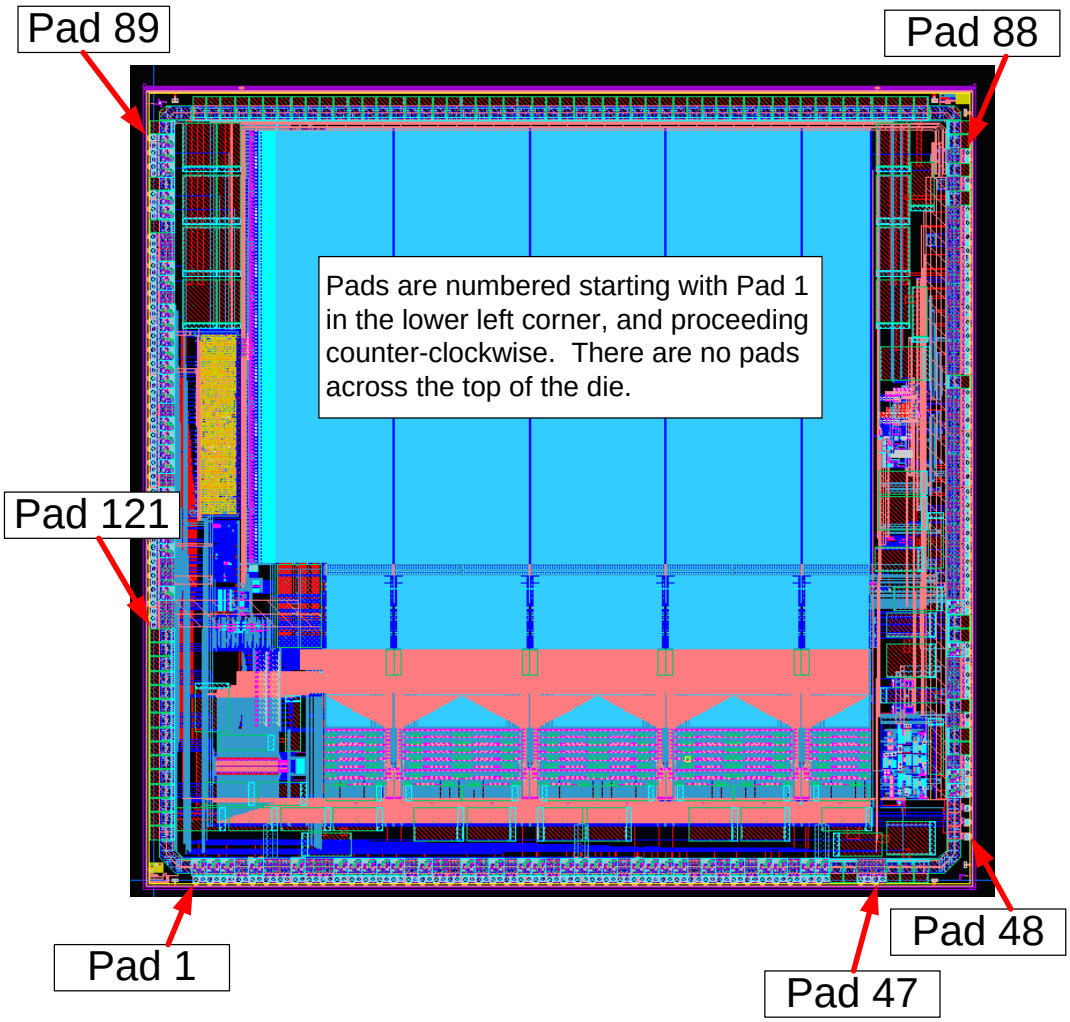
Figure 1: HTEEPROM Die Functional Block Diagram



KEY

- Serial / Parallel Control and Configuration Protect Input
- 28C256 Functionally Equivalent Parallel Interface
- 25C256 Functionally Equivalent Serial Interface
- High Temperature FPGA Configuration Interface
- Periodic Refresh Request Timer and Handshake Control
- External Ceramic Chip Capacitors Support Charge Pumps For Write Operations

Figure 2: HTEEPROM Die Pad Numbering and Orientation



Pad Number	Signal Name
1	OEN
2	WEN
3	CSN
5	ERRN
8	SELSNP
11	TM_NPOE
12	SCK
13	SI
14	WPN
15	HOLDN
17	SBP0
20	SBP1
22	SO
24	TM_NSAEN
25	TM_NCSALL
27	D0
28	D1
29	D2
30	D3
32	D4
33	D5
34	D6
35	D7

Pad Number	Signal Name
37	CHECKN
39	CCLK
41	CONN
42	PORINN
44	TM_ECC_NDISABLE
45	TM_ECC_FLAG
46	TMPDIOD
48	VBG
49	NOK
50	VREF
51	TM_FG_REF_NOE
52	TM_VRBUFF_OE
54	VMRAMP
58	TM_DIOD_NEN
59	TM_HYS_NEN
60	FG_REF
63	NGATE
64	PGATE
65	VPRAMP
67	CM4_M
68	CM3_M
69	CM13_P
71	CM2_M

Pad Number	Signal Name
72	CM2_P
73	CM1_M
75	CP3_P
76	CP2_M
78	CP2_P
79	CP1_M
80	CP1_P
82	VP
83	VM
85	VREF15
86	IREF10UA
88	CDRV
89	TM_NZVTST
90	TM_NRFSHOSC
91	TM_NRFSHDIV
92	NRFSHRQ
93	NRFSHACK
96	TM_NSELALL
97	TM_NSELHALF
99	A0
100	A1
101	A2
102	A3

Pad Number	Signal Name
103	A4
104	A5
105	A6
107	A7
108	A8
109	POROUTN
110	A9
112	A10
113	A11
114	A12
115	A13
116	A14
119	CFG_PROT

VDDA Pads
61
87

VSSA Pads
62
84

VDD Pads
4
6
7
18
21
23
31
38
40
43
53
56
70
77
94
95
106
117
118

VSS Pads
9
10
16
19
26
36
47
55
57
66
74
81
98
111
120
121

TABLE 1:HTEEPROM Pad Types:

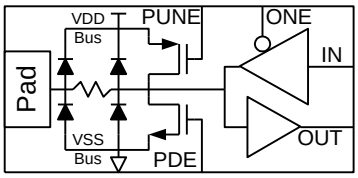
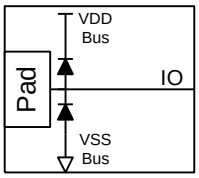
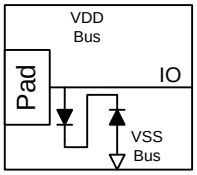
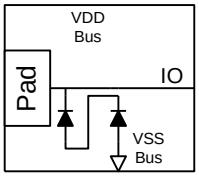
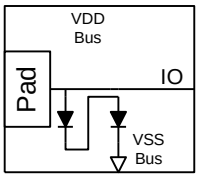
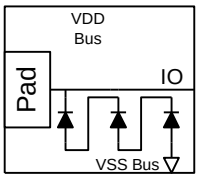
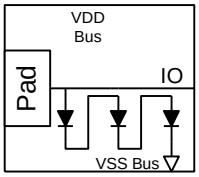
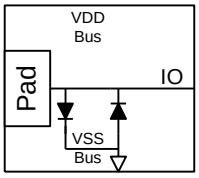
Pad Type	Layout Cell Name	Max. Voltage Range	ESD Configuration
D	bipad_dig **ALL USER I/O are this pad type.**	VDD+V(diode) VSS-V(diode)	
A	esd_ana_rthru	VDD+V(diode) VSS-V(diode)	
APM	esd_pos_neg	VSS+ ~7 V +V(diode) VSS- ~7 V -V(diode)	
HVP	esd_hv_pos	VSS+ ~14 V VSS-2xV(diode)	
HVM	esd_hv_neg	VSS+2xV(diode) VSS- ~7 V -V(diode)	
HVP3	esd_hv3_pos	VSS+ ~21 V VSS-3xV(diode)	
HVM3	esd_hv3_neg	VSS+3xV(diode) VSS- ~21 V	
AG	esd_vssa	0V VSSA	

TABLE 1:HTEEPROM Pad Types:

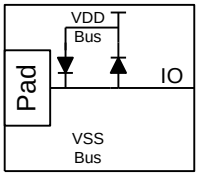
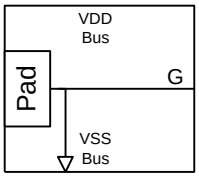
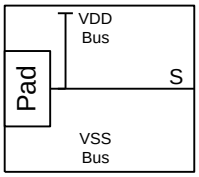
Pad Type	Layout Cell Name	Max. Voltage Range	ESD Configuration
AS	esd_vdda	5V (typ.) VDDA	
G	esd_vss_pwr_pad	0V VSS	
S	esd_vdd_pwr_pad	5V (typ.) VDD	
TP	Test point		No schematic. This is just a signal routed directly to a pad for test evaluation only. No ESD protection is provided.

Table 2: HTEEPROM Power/Ground Pad List:

Supply: Voltage	Pad Type	Pad Number(s)
VDD: Primary power = 5V (typical)	S	4, 6, 7, 18, 21, 23, 31, 38, 40, 43, 53, 56, 70, 77, 94, 95, 106, 117, 118
VSS: Primary ground connection = 0V	G	9, 10, 16, 19, 26, 36, 47, 55, 57, 66, 74, 81, 98, 111, 120, 121
VDDA: Analog power = 5V (typical)	AS	61, 87
VSSA: Analog ground connection = 0V	AG	62, 84

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
A<14:0> A14: 116 A13: 115 A12: 114 A11: 113 A10: 112 A9: 110 A8: 108 A7: 107 A6: 105 A5: 104 A4: 103 A3: 102 A2: 101 A1: 100 A0: 99	Parallel mode: Input only Serial Mode: See functional description	Address Parallel mode: - inputs address to parallel digital block. - A<14:6> select 1 of 512 rows (pages). - A<5:0> select 8 of 512 columns (1 byte of 64 bytes within page). - input address is latched on falling edge of CEN or WEN, whichever occurs last. Serial mode: Function depends upon TM_NPOE (TM_NPOE is normally =1). - TM_NPOE = 1, configured as inputs with active pull-ups. - TM_NPOE = 0, configured as outputs (pull-ups disabled). In this mode, A<14:0> monitors addresses passed from SPI to the parallel block.

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
D<7:0> D7: 35 D6: 34 D5: 33 D4: 32 D3: 30 D2: 29 D1: 28 D0: 27	Parallel mode: Bidirectional Serial Mode: See functional description	Data I/0 Parallel mode: - data input/output, 8 bits. - data page is 64 bytes (512 bits); the specific byte within page is set by A<5:0>. - output when WEN is high, AND both CSN and OEN are low. - input when CSN AND WEN are low, and OEN is high. - input data is latched on rising edge of CSN OR WEN, whichever occurs first. - D<7>, Data Polling indicates completion of write cycle Attempting to read the last byte written will output the complement on D<7> until the write cycle is complete. - D<6>, Toggle Bit. While a write cycle is in progress, reading data will result in D<6> toggling between 1 and 0. Serial mode: Dependent upon TM_NPOE. (TM_NPOE is normally =1). - TM_NPOE = 1, configured as inputs with active pull-ups. - TM_NPOE = 0, configured as outputs (pull-ups disabled). In this mode, D<7:0> monitors data read out of memory array at location determined by A<14:0>. There is no option to monitor data being written into array.
CSN: 3	Input	Chip Select, Active Low (0) - same pad used for both parallel and serial mode to enable/select chip. - chip selected when pulled low. Serial mode: - 1 to 0 transition required prior to any sequence. - 0 to 1 transition after valid write sequence initiates internal write.

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
OEN: 1	Parallel mode: Input Serial Mode: See functional description	Output Enable, Active Low (0) Parallel mode: - enables D<7:0> pads to output selected data by A<14:0> during read operation. - must be activated along with CEN, see 28C256 timing. Serial mode: Dependent upon TM_NPOE (TM_NPOE is normally =1). - TM_NPOE = 1, configured as inputs with active pull-ups. - TM_NPOE = 0, configured as outputs (pull-ups disabled). In this mode, configured as output that monitors internal OEN signal from SPI port to parallel digital block. Will change in real time with internal OEN signal from SPI to parallel digital block.
WEN: 2	Parallel mode: Input Serial Mode: Output	Write Enable, Active Low (0) Parallel mode: - enables D<7:0> pads to input data during write operation. - must be activated along with CEN, see 28C256 timing. - page writing accomplished using pulses on WEN. A<14:6>, page address, latched on last falling edge of WEN. Serial mode: Dependent upon TM_NPOE. (TM_NPOE is normally =1). - TM_NPOE = 1, configured as inputs with active pull-ups. - TM_NPOE = 0, configured as outputs (pull-ups disabled). In this mode, configured as output that monitors internal WEN signal from SPI port to parallel digital block. Will change in real time with internal WEN signal from SPI to parallel digital block.
CFG_PROT: 119	Input	Configuration Protection Can be used to protect FGPA configuration that may be stored in the lower half of memory. 1 = Lower half of memory blocked from being written. 0 = All of memory available for write.

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
SELSNP: 8	Input	Product Interface Mode: Select Serial NOT Parallel: 0 = Parallel 1 = Serial Parallel mode - CSN, OEN, WEN, A<14:0>, D<7:0> interface with product. - Pads CSN, SCK, SI, WPN, HOLDN are configured as inputs with active pullups enabled, held to logic 1. Serial mode: - Mode (inputs or monitoring outputs) of A<14:0>, OEN, WEN, D<7:0> determined by TM_NPOE (TM_NPOE is normally high) - CSN, SCK, SI, WPN, HOLDN interface with the product. Output data is supplied on SO.
SO: 22	Output	Serial Data Output Serial Mode: - During a read cycle, data is shifted out on falling edge of SCK. - Tristate when CSN is 1. - Tristate when HOLDN is 0, and CSN is 0. Parallel Mode: - Configured as output with static logic 0.
SI: 13	Input	Serial Data Input Serial Mode: - Op codes, byte address and data to be written latched on rising edge of SCK Parallel Mode: - Input with Active Pull Up enabled.

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
SCK: 12	Input	Serial Clock Serial Mode: - Op codes, byte address or data present on SI pin latched on rising edge. - Data on SO updated on falling edge. Parallel Mode: - Input with Active Pull Up enabled.
WPN: 14	Input	Write Protect, Active Low (0) Serial Mode: - When tied low, 0, and WPEN bit in the status register is set to 1, all write operations to the status register are inhibited. - WPN going low while CSN is low will interrupt a write to the status register. - WPN going low after an internal write cycle has begun will have no effect on any write operation to the status register. - WPN function is block when WPEN bit is set to 0. Parallel Mode: - Input with Active Pull Up enabled.
HOLDN: 15	Input	Hold/Pause of serial transmission, Active Low (0) Serial Mode: - Pause transmission while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. - To pause, HOLDN must be brought low while SCK is low. - SO pin goes to tristate when paused. - Transitions on SI are ignored Parallel Mode: - Input with Active Pull Up enabled.

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
SBP0: 17	Input	Serial Mode Block Protect Bit 0 Serial Mode: - Set the initial state of the BP0 bit in the status register upon POR. - State of bit can then be changed via WRSR operation. - Can be tied off to adjacent VDD pad Parallel Mode: - Input with Active Pull Up enabled.
SBP1: 20	Input	Serial Mode Block Protect Bit 1 Serial Mode: - Set the initial state of the BP1 bit in the status register upon POR. - State of bit can then be changed via WRSR operation. - Can be tied off to adjacent VDD pad Parallel Mode: - Input with Active Pull Up enabled.
CCLK: 39	Input	FPGA Configuration Clock Parallel Mode: - input clock generated by FPGA, used to load data into FPGA - typically 1 MHz - FPGA will sample data outputs D<7:0> on rising edge Serial Mode: - Configured as input, can be tied off to adjacent VDD pad
ERRN:5	Parallel mode: Bidirectional Serial Mode: Input	FPGA Data Validation Error, Active Low (0) Parallel Mode: - used along with CHECKN to manage data validation in FPGA - initially an input from FPGA when validation fails. - if validation fails a second time, is latched and output by EEPROM. Serial Mode: - Configured as input, can be tied off to adjacent VDD pad

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
CHECKN: 37	Output	FPGA Data Validation Signal, Active Low (0) Parallel Mode: - used along with ERRN to manage data validation in FPGA SRAM - timed with CONN to trigger data validation cycle. - CHECKN is always enabled with FPGA configuration to trigger data validation, it is not optional. Serial Mode: - Configured as output with static logic 0.
CONN: 41	Parallel mode: Bidirectional Serial Mode: Input (with pull-up)	FPGA Configuration Control, Active Low (0) Parallel Mode: - Open Drain Output, with active pull up - After FPGA boot sequence, configuration initiated by pulling CONN low. Serial Mode: - Configured as input with pull up.
NRFSHRQ: 92	Output	Request to begin EEPROM Data Refresh, Active Low (0) - output to external system indicating need to refresh EEPROM data - after initiating, wait for acknowledgement on RFSHACK before starting refresh operation. - after receiving RFSHACK, remains high until refresh of entire memory is complete.
NRFSHACK: 93	Input	Acknowledgement of Refresh Request, Active Low (0) - input from external system indicating that it is prepared for the EEPROM to become unavailable while data refresh is performed. - can be a pulse, or remain high for the entire duration of RFSHREQ. - after receiving the acknowledgement, EEPROM will complete any in-progress IO or internal writes and then ignore external IO requests until refresh is complete.
POROUTN: 109	Output	POR Output, Active Low (0) - indicates that supply on EEPROM is too low for proper operation. - internally, it is combined with PORNINN to generate internal POR - expected to be connected to RESETN input of FPGA. - all digital logic is held in a reset state, the refresh timer is reset.

Table 3: HTEEEPROM Pad List: User I/O

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Serial vs. Parallel mode operation is determined by SELSNP input (Low = parallel, High = Serial)

Name: Pad #	Configuration	Functional Description
PORINN: 42	Input with Pull-up	POR Input, Active Low (0) - expected to be used with FPGA pin POROUTN - indicates that supply on FPGA is too low for proper operation.

Table 4: HTEEPROM Analog Functional and/or Analog Test/Observation Pads

Name: Pad #	Pad Type	Functional Description
Positive Charge Pump Capacitor Terminations		Charge pump is active only during writing to the HTEEPROM. Otherwise voltage across capacitors is in the range of VSS to VDD. These terminals are not brought out to package pins.
CP1_P: 80	A	1st Stage Capacitor, Positive Terminal (voltage = VDD to 2xVDD)
CP1_M: 79	A	1st Stage Capacitor, Minus Terminal (voltage = VSS to VDD)
CP2_P: 78	HVP	2nd Stage Capacitor, Positive Terminal (voltage = 2xVdd to 3xVDD)
CP2_M: 76	A	2nd Stage Capacitor, Minus Terminal (voltage = VDD to 2xVDD)
CP3_P: 75	HVP3	3rd Stage Capacitor, Positive Terminal (voltage ≈ 3xVDD). Minus terminal is connected to VSS.
Negative Charge Pump Capacitor Terminations		Charge pump is active only during writing to the HTEEPROM. Otherwise voltage across capacitors is in the range of VSS to VDD. These terminals are not brought out to package pins.
CM13_P: 69	A	1st and 3rd Stage Capacitor, Positive Terminal (voltage = VSS to VDD)
CM1_M: 73	APM	1st Stage Capacitor, Minus Terminal (voltage = VSS to -VDD)
CM2_P: 72	A	2nd Stage Capacitor, Positive Terminal (voltage = VSS to VDD)
CM2_M: 71	HVM	2nd Stage Capacitor, Minus Terminal (voltage = -VDD to -2xVDD)
CM3_M: 68	HVM3	3rd Stage Capacitor, Minus Terminal (voltage = -2xVDD to -3XVDD)
CM4_M: 67	HVM3	4th Stage Capacitor, Positive Terminal (voltage ≈ 3x VDD). Minus terminal is connected to VSS.
VP: 82	HVP	Positive High Voltage Supply (regulated supply for HTEEPROM Write) - primarily for test access / observation Typically, this signal sits at VDD when not performing an internal write. During an internal write, this signal will provide a higher regulated voltage, approx. 8.25 V.

Table 4: HTEEPROM Analog Functional and/or Analog Test/Observation Pads

Name: Pad #	Pad Type	Functional Description
VM: 83	HVM	Negative High Voltage Supply (regulated supply for HTEEPROM Write) - primarily for test access / observation Typically, this signal sits at VSS when not performing an internal write. During an internal write, this signal will provide a regulated voltage of approx. -8.25 V.
VPRAMP: 65	HVP	Positive Ramp Waveform: Applied during HTEEPROM Write - primarily for test access / observation This signal carries both the memory cell read voltage and high-voltage waveforms used during writing. The memory cell read voltage buffer can be disabled so that an external read voltage can be applied to this pad. However, the range of read voltages applied to this node is limited by two PMOS transistors in the high voltage interface. To inject larger read voltage variations, look into applying signal to CDRV. The read voltage that appears on VPRAMP should be (1/0.846) * FG_REF.
VMRAMP: 54	HVM	Negative Ramp Waveform: Applied during HTEEPROM Write - primarily for test access / observation
FG_REF: 60	A	Sense Amp Read Voltage Reference. Provides access to the internal FG_REF signal. The FG_REF signal will only be routed to this pad when TM_FG_REF_NOE = 0. Otherwise, this pad is floating. - This pad is not used in normal operation. It is made available for diagnostic monitoring or adjustment of a reference voltage used in the sense amplifiers when reading data.
IREF10UA: 86	A	Reference Current Monitor Output. - This pad is not used in normal operation. It is a replica of an internally generated reference current (out of VDDA). It is nominally 10uA.
VREF15: 85	A	Buffered 1.5 Reference Voltage - This pad is not accessed in normal operation. It is available to measure/test the output of an internal voltage reference (VREF block) and may be used during VREF trim at wafer level probe (if necessary)

Table 4: HTEEPROM Analog Functional and/or Analog Test/Observation Pads

Name: Pad #	Pad Type	Functional Description
TMPDIOD: 46	AG	On-Die Temperature Diode Comprised of two parallel diodes connected to VSS. Current can be forced into, or out of, this pad and the resulting voltage measured to determine die temperature.
CDRV: 88	APM	Directly Applied Read Voltage - Input with internal pull-down - This pad is not used in normal operation. It is provided to enable direct manipulation of read voltages applied to the control capacitor of selected memory rows, for diagnostic test purposes. Application of the voltage on CDRV to the memory rows is controlled by the PGATE and NGATE inputs.
PGATE: 64	APM	Control for PDMOS switches that apply CDRV to selected memory rows. . - Input with internal pull-down - Leave this pad unconnected (or un-driven) for normal operation. - Used in conjunction with NGATE switch - To connect CDRV to memory rows, pull PGATE to -5V. Otherwise pull PGATE to VSS, or leave unconnected - NDMOS switches are in series with PDMOS switch, thus both must be turned on to connect C_DRV to the rows. (See NGATE)
NGATE: 63	APM	Control for NDMOS switches that apply CDRV to selected memory rows. . - Input with internal pull-down - Leave this pad unconnected (or un-driven) for normal operation. - Used in conjunction with PGATE switch - To connect CDRV to memory rows, pull NGATE to +5V. Otherwise pull NGATE to VSS, or leave unconnected - NDMOS switches are in series with PDMOS switch, thus both must be turned on to connect C_DRV to the rows. (See PGATE)
VREF: 50	TP	Test point for un-buffered voltage reference VREF. Expected value is ~1.5V. For wafer probe only. This terminal is not brought out to a package pin.

Table 4: HTEEPROM Analog Functional and/or Analog Test/Observation Pads

Name: Pad #	Pad Type	Functional Description
NOK: 49	TP	Test point for voltage reference "Not OK" (NOK signal). This is a digital signal indicating proper start-up of the vref circuits: 0 – voltage reference is active and should be valid 1 – voltage reference is disabled or has an error For wafer probe only. This terminal is not brought out to a package pin.
VBG: 48	TP	Test point to monitor internal voltage reference signal VBG. Expected value is ~2.43V. This signal comes directly from vref_gen2 block. In the event that the internal voltage reference fails, this pad can be used as an input to override the internal voltage reference. For wafer probe only. This terminal is not brought out to a package pin.

Table 5: Digital Test/Configuration Pads

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Name: Pad #	Configuration	Functional Description
TM_NSELALL: 96	Input (with pull-up)	Select All Rows Test Mode, Active Low (0) - allows all 512 rows to be selected for internal write. Data written into page buffer is written into all rows during the internal write.
TM_NSELHALF: 97	Input (with pull-up)	Select Half of All Rows Test Mode, Active Low (0) - allows either all the ODD or EVEN rows to be selected for internal write. Address bit A<6> determines whi.
TM_NCSALL: 25	Input (with pull-up)	Select All Columns Test Mode, Active Low (0) - allows 512 bit page register to be loaded in one setup by repeating the 8 bits presented at D<7:0> 64 time across the 512 bit page. - bypasses page byte address selected by A<5:0>. - only applicable when loading the data latches from data input at D<7:0>, prior to performing an internal write. NOTE: The data stored in the data latches then serves the column interfaces by providing DATA and NDATA signals that control the column interface with Programming/Erasing the data into the memory array.

Table 5: Digital Test/Configuration Pads

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Name: Pad #	Configuration	Functional Description
TM_NSAEN: 24	Input (with pull-up)	Sense Amplifiers Test Mode, Active Low (0) - enables all 512 (one for each column) sense amplifiers and prepares their Global Bit Line (GBL) input to accept current from the memory array. - use in conjunction with A<14:6> and read mode to select the row (page) of data to read, and connect that row to the GBL. - A<5:0> then determine which 8 of the 512 page bits are available at the D<7:0> output. NOTE: Under normal product operation, sense amplifiers are only enabled long enough to read the data from memcells (say 100 to 200 ns). This test mode continuously enables the sense amplifiers. This allows for test modes during which the sense amp reference or memcell read voltage is varied to determine the memory cell's threshold shift. When performing continuous sense amplifier testing, it may also be of value to enable the TM_HYS test mode to avoid toggling the sense amplifiers while sweeping.
TM_ECC_NDISABLE: 44	Input (with pull-up)	ECC Disable Test, Active Low (0) 0 = ECC disabled. 1 = ECC enabled, normal product operation.
TM_ECC_FLAG: 45	Output	ECC Active Flag 1 = ECC was utilized in the most recent read operation. 0 = ECC has not been utilized.
TM_HYS_NEN: 59	Input (with pull-up)	Disables Sense Amp Hysteresis, Active Low (0) - adds about 6-7 % of hysteresis to the sense amp detection. - useful in avoiding toggling of the sense amplifier outputs when varying the memory cell read voltage, or the sense amplifier references, in attempts to measure the memory cell threshold shift/stored charge.

Table 5: Digital Test/Configuration Pads

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Name: Pad #	Configuration	Functional Description
TM_VRBUFF_OE: 52	Input (with pull-up)	VRMEM Buffer Enabled Allows the buffer between VRMEM (memory cell read voltage) and VPRAMP to be disabled so that VPRAMP can be driven externally with a different read voltage. 1 = Buffer is enabled, and controlled internally by NWRITE 0 = Buffer is disabled, and disconnected from VPRAMP.
TM_DIOD_NEN: 58	Input (with pull-up)	Disables GBL Voltage Reduction, Active Low (0) - causes voltage of the Global Bit Line (GBL) input of the sense amplifiers to be reduced during read operations. NOTE: The body-source diode of the NMOS FET in the sense amplifiers input inverter is forward biased with a small current. This reduces the threshold voltage of the NMOS FET, which reduces the GBL voltage when sensing current from the memory array. The GBL voltage is also the voltage at the drain of the memcell output. When reading the memory, the memcell carries current. Depending on the current, and the resulting drain voltage, there may be a chance that hot electrons (high energy carriers) are generated that could then tunnel through the memcell FET's gate oxide and affect charge stored on the floating gate ... thus upsetting the memory's ability to store data. By reducing the voltage at the GBL, this may reduce the generation of hot electrons. It is not yet known the potential impact or need for this feature. It is only included for development characterization.
TM_NRFSHOSC: 90	Input (with pull-up)	Refresh Oscillator Test, Active Low (0) Clock used to drive 30 second counter is output on NRFSHRQ. Approx. frequency, just less than 3 kHz.
TM_NRFSHDIV: 91	Input (with pull-up)	Refresh 30 Day Counter Test, Active Low (0) Allows for fault coverage of flip-flop chain that makes 30 day counter. NRFSHRQ will output a specific pattern that will verify the flip-flops that build the counter chain.
TM_FG_REF_NOE: 51	Input (with pull-up)	FG_REF Output Control, Active Low (0) Enables the internal signal FG_REF to be connected to FG_REF pad for observation.

Table 5: Digital Test/Configuration Pads

All user pads listed in this table are Pad-type "D" (Bi-directional Digital I/O Pad)

Name: Pad #	Configuration	Functional Description
TM_NPOE: 11	Input (with pull-up)	Parallel Outputs Enable, Active Low (0) Allows parallel product pads to be configured as outputs when operating in serial mode. When SELSNP = 1 (serial mode), this pin enables A<14:0>, D<7:0>, WEN, OEN to be configured as outputs that monitor the internal signals going between the serial and parallel blocks.
TM_NZVTST: 89	Input (with pull-up)	Zero Volt Read Test, Active Low (0) Allows the read voltage applied to the C node of the memory cells to be forced to 0 V. Has potential application in data retention testing. Normally, the memory cell read voltage applied to VPRAMP is passed through the high voltage row interfaced to the C node of the associated row. When NZVTST is pulled low, it disables this path through the row interface and pulls the C node to VSSA.

HiTEN 2007 Paper

"Updated Results from Deep Trek High Temperature Electronics Development Programs"

APPENDIX to
Final Report

Deep Trek
Re-configurable Processor for Data Acquisition (RPDA)

Honeywell

Updated Results from Deep Trek High Temperature Electronics Development Programs

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Introduction

Electronics are used in modern oil and gas exploration to collect, log, and/or process data such as heading and inclination, weight on the bit, vibration, seismic/acoustic response, temperature, pressure, radiation, and resistivity of the strata. High-temperature electronics are needed that can reliably operate in deep-well conditions (up to 250°C). The U.S. Department of Energy Deep Trek program has funded two projects led by Honeywell. The first project, launched in 2003 and completed this year, established a production-level integrated circuit (IC) manufacturing process, components and design tools [1-4] specifically targeting high-temperature environments (up to 250°C). The second project, launched in 2006 and completing in 2008, will develop rugged packaging suitable for down-hole shock and vibration environments which will be used to house and demonstrate components developed in the earlier project. This paper describes updated results of these successful projects.

Deep Trek Projects

Oil and gas drilling time and costs escalate when the target reservoir is very deep. Relative to more conventional well depths it is therefore even more important to be able to monitor down-hole conditions in deep wells (>15,000ft, 4,575m). This creates a catch-22 situation because electronics that can reliably operate in deep-well conditions have not been available, primarily due to the high temperature (up to 250°C, 481°F) encountered at great depth. Commercial electronics are not designed for these temperatures, and conventional integrated circuit (IC) technology is not capable of operating at these temperatures. To help overcome this limitation, the U.S. Department of Energy Deep Trek program has funded two projects led by Honeywell to develop electronic components that can handle the heat and deliver the data operators need to undertake deep-reservoir development.

The first project, launched in 2003 and completed this year, established a production-level IC manufacturing process along with IC design tools (software and simulation elements) specifically targeting high-temperature environments. These IC technology and design tools were then employed to develop prototype high-temperature IC components, with the objective that these will be made available to the industry as commercial products. This project was completed in collaboration with a Joint Industrial Participation (JIP) consortium of commercial partners. The JIP partners defined priorities and specifications for components developed and demonstrated within the project. These include:

- a dual precision amplifier,
- a field programmable gate array (FPGA),
- a high-resolution A-to-D converter,
- a high-temperature non-volatile memory (EEPROM).

An additional outcome of this project is a family of metal mask programmable gate-arrays suitable for use up to 250°C.

The second project, launched in 2006 and scheduled for completion in 2008, will develop rugged multi-chip-module (MCM) packaging suitable for down-hole shock and vibration environments. An MCM package developed under this project will be used to house and demonstrate components developed in the earlier project.

High Temperature Wafer Process Technology

A partially depleted 0.8 micron SOI CMOS IC manufacturing process has been developed and established in factory production specifically for high-temperature applications [5]. The wafer process flow was adapted from a previously established SOI technology in use for aerospace products. This adapted technology has been successfully applied in the

manufacture of all of the proto-type IC components within these Deep Trek projects. All of the devices in this process are suitable for long-term operation (5 years at 225°C) using 5V supplies. Besides the use of SOI structure, the primary feature of the wafer process to address high temperature includes the adjustment of transistor threshold voltages to minimize sub-threshold leakage. Up to four layers of aluminium interconnect are available. Inter-connect electro-migration reliability is established by characterization and adherence to design rules limiting the maximum current density in the conductors, either through de-rating of operating frequency (for digital applications) or through high temperature optimized interconnect layout (primarily power bus and/or DC output conductors). Analog elements (CrSiN thin-film resistors, MOS capacitors, and lateral PNP transistors) are available and supported.

Temperature-compensated biasing techniques for analog circuits are employed to maintain gain and bandwidth over an extremely wide temperature range. Design toolkits have been updated and applied for high temperature applications. These include development of SPICE models applicable from -55°C to 250°C.

Purely analog (or full-custom digital) blocks are implemented using traditional analog tools and processes, including schematic entry and SPICE based simulation methodologies. This is done using a Process Design Kit (PDK) which is an integrated collection of schematic capture symbols, models, layout rules, and other items to allow use of design software available from Cadence. Laser-trimming and high temperature wafer probing can be combined to adjust voltage reference temperature coefficients, or for tailoring other temperature-dependent circuit performance.

Now that the first Deep Trek project has been completed this wafer process, layout rules, SPICE models, and Cadence design and layout toolkit items may be accessed on a foundry basis.

High Temperature Digital Gate Arrays and Design Infrastructure

Digital functions are commonly defined at a behavioural level in the form of hardware description language (HDL) netlists. Once defined by this means they are commonly implemented in hardware by a process of synthesis into a gate-level structure which is then fabricated using gate-array IC platforms. A family of metal-mask programmable gate arrays suitable for manufacture in the 0.8 micron SOI process (described above) has been validated for high-temperature use. This gate-array family (HT2000) uses established HDL-based development tools and flows [6, 7]. The conventional Honeywell design tools and techniques have been extended for high-temperature application. This includes simulation timing models that are applicable at 250°C, and load-checking routines for adherence to rules appropriate to address high-temperature electro-migration concerns. The HT2000 family of high-temperature gate-arrays incorporates a family of die encompassing a ranging from 27,000 to 275,000 usable gates. For ASIC designs incorporating a mix of analog and digital blocks, sub-modules of analog and/or custom digital circuitry may be embedded inside the gate-array I/O ring. For example, this was the means for implementing one of the high-temperature A-to-D converters in this project.

Dual Precision Amplifier

A high-temperature dual precision amplifier has been developed and fully-verified at 225°C with additional testing up to 375°C [8]. The component die size is 2.3mm x 1.8mm. The amplifier is continuously auto-zeroed to achieve very low offset and low-frequency noise, making it suitable for low-frequency DC-coupled sensor-interface applications. The auto-zero function requires a clocking source. The chip can provide this clock autonomously via an on-chip oscillator, or there is the option of providing an off-chip clock. Using an off-chip clock can provide more optimal performance, especially for sampled-data systems where usage of an off-chip clock can allow synchronization with the sampling period. The dual precision amplifier also has a sleep-mode feature to conserve power when the amplifier is not in use. Previously reported data from prototype characterization is summarized in Table 1 below. Manufacturing test programs have been developed and test/assembly flows have been established for commercial sales in the form of 14-pin DIP packages or as deliverable die.

TABLE 1 : Dual Precision Amplifier Packaged Test Data (-55°C to 225°C) unless noted

Parameter	Target Value	Measured Results
Input Offset Voltage	±100 μV (max.)	±5 μV (external clock)
Supply Current (5.25V supply, 225°C)	5 mA	1.85 mA
Open-loop Gain (-55°C to 225°C)	> 100dB	> 114dB
Input Noise Voltage RS=100Ω, 0.1Hz – 10Hz (internal clock) (External clock at 30KHz)	 3 μV pk-pk	5.7 μV pk-pk @ 23°C 4.6 μV pk-pk @ 225°C 1.4 μV pk-pk @ 23°C
Input Range	V_{SS} to V_{DD} -2.0	V_{SS} to V_{DD} – 1.7
Output Source/Sink (swing to 0.3V from either rail)	±20 mA	> 20 mA
Output Short-Circuit Current Limit	±50 mA	51 mA (average)
Supply Current with Shutdown asserted	150 μA, maximum	13 uA, typical

High-temperature Field Programmable Gate Array

Low-volume digital IC applications are often addressed by the use of programmable logic devices. These go by a variety of names, including Field Programmable Gate Arrays (FPGAs). FPGAs apply the economic advantages of batch processing to low-volume or application-specific digital components by enabling the user to customize components on a unit-by-unit basis. An FPGA is configured by electrical means, such as writing to configuration memory (in the case of a reconfigurable FPGA) or else by a process of permanently configuring the part by electrical fusing.

FPGA products are not commercially available for the extreme high temperature environment (at or above 225°C) required by the Deep Trek program. Therefore, a high-temperature FPGA has been developed under the Deep Trek program. It is a licensed functional equivalent to a commercial FPGA, the Atmel AT6010 [9]. The high temperature FPGA has been designed using the HTSOI process for specified operation at 225°C. It is a re-programmable, SRAM-based FPGA that provides 30,000 programmable logic gates and 204 programmable inputs/outputs. Configuration is controlled by dedicated configuration pins and dual-function pins. Dual function pins double as user I/O pins after the device is configured and in operation [10]. The devices can be partially reconfigured while in operation; where portions of the device not being modified remain operational during reconfiguration. The high-temperature FPGA has been fully verified by wafer-probe testing at 200°C (391°F). The design includes more than 3 million transistors, yet standby leakage current at 200°C is still under 0.5mA. This design will be offered in die-form, as well as embedded within the RPDA multi-chip module described later.

High-temperature A-to-D Converters

Two complete high-temperature A-to-D converters have been proto-typed. The first, a high-resolution A-to-D was funded under the Deep Trek program [4]. The second, a 12-bit successive-approximation A-to-D was completed in parallel with the Deep Trek program. A comparison of features and performance is provided in Table 2.

The Deep Trek A-to-D was developed to digitize DC and very-low frequency signals to a high level of resolution. The design provides 20-bits of resolution, although effective performance was not expected beyond 18-bits. The Deep Trek program intent is to develop a high-resolution A-to-D (targeting 18-bit performance) suitable for industry use as a commercial product (referred to as HTADC18). A block diagram of the HTADC18 is shown in Figure 1. The core A-to-D function is provided by a 2nd-order sigma-delta modulator with a single-bit output at an over-sampling ratio of 2048 (single-bit modulator output rate is 204.8KHz). An on-chip digital decimation and filter processes the modulator output to develop a 20-bit conversion result at 100 samples per second. Other features include a Reference and PTAT (Proportional-To-Absolute Temperature) block [11]. This block generates voltage-reference and current-reference outputs, as well as a PTAT current source, and a "thermometer" voltage. The thermometer voltage was designed for use as an on-chip temperature monitor. The HTADC18 also includes an auxiliary 8-bit successive approximation A-to-D which can be used to digitize either this temperature signal or an external signal source depending on the user's preference. The HTADC18 incorporates a self-contained oscillator so that the A-to-D can function autonomously, and a serial I/O block (Serial Peripheral Interface, or SPI). Using the SPI the HTADC18 can be configured to operate in several modes, or be placed into sleep state to minimize power consumption when not in use. Also via the SPI the HTADC18 can be configured so that the raw modulator output and 204.8KHz sampling clock are available on the MDO and CLKOUT pins respectively. This last feature enables potential use with external decimation and filtering functions that might be employed to achieve faster update rates at the price of overall resolution.

TABLE 2 : High-temperature A-to-D Converter Features and Prototype Performance

Feature	Deep Trek High-Resolution A-to-D	12-bit A-to-D
Output Resolution	20 bits	12 bits
Architecture	2nd order sigma-delta	Successive Approximation
Update Rate	100 Samples/sec	100K Samples/sec
Input	Differential (with single-ended option)	Single-ended
Output format	Serial	Parallel
DC Linearity at 225°C	16.7 bits	10.7 bits
Power Dissipation at 225°C	35mW	*No data at this time*
ENOB at 225°C	17.4 bits	
Output repeatability	17.7 bits (RMS), 15 bits pk-to-pk	
Die Size	10.4 mm x 9.5 mm	3.2 mm x 2.8mm
Prototype Package Configuration	28-pin DIP	28-pin DIP

The HTADC18 was implemented by partitioning the design between analog functions (oscillator, modulator, 8-bit ADC, Reference and PTAT block) and digital functions (digital filter and serial data interface). Analog functions were collected into a single analog/mixed-signal block and dropped into a high-temperature gate-array die which contains all digital functions. Digital blocks are synthesized from behavioural HDL using the high-temperature HT2000 toolkit and design platform.

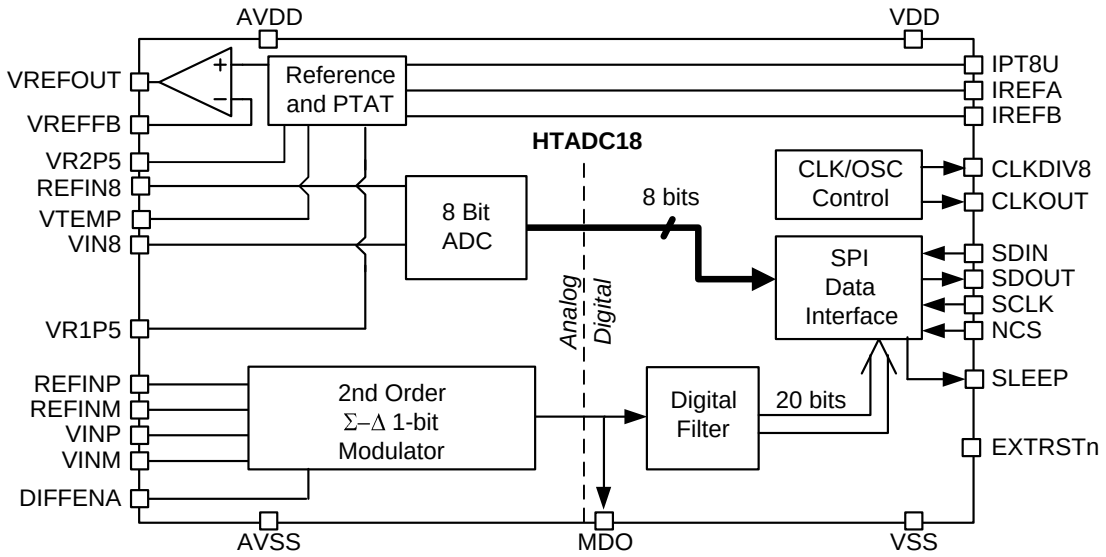


FIGURE 1: Deep Trek High-Resolution A-to-D (HTADC18) Block Diagram

Two design iterations of the HTADC18 have been completed. After a final assembly process flow is developed the HTADC18 will be capable for commercial sale in a 28-pin DIP package.

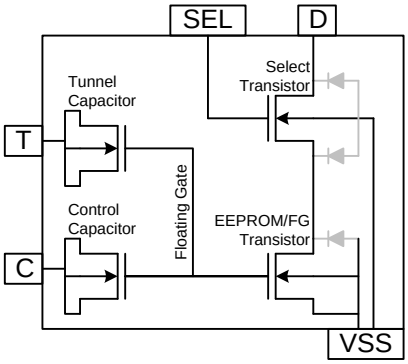
The 12-bit A-to-D converter is a successive approximation A-to-D based using an embedded capacitive charge re-distribution DAC. This recently fabricated design is an extension to 12-bit resolution of the auxiliary 8-bit ADC that is embedded within the Deep Trek HTADC18. Prototype evaluation over temperature shows a repetitive non-linearity that occurs with every 64 output codes. This is most likely caused by a systematic matching error in the capacitor array of the DAC. Including this error, overall linearity is within plus/minus 2.5 LSB's. This should be easily improved to plus/minus 1.5 LSB's assuming that the systematic DAC error can be identified and eliminated.

High-temperature EEPROM

A high-temperature non-volatile memory was one of the chief component objectives of the Deep Trek High-Temperature Electronics program. The resulting high-temperature EEPROM (HTEEPROM) development was logistically constrained to an approach that could be implemented in the Deep Trek HTSOI wafer process flow with no

additional processing steps. For this reason a single-poly floating gate structure was chosen as the basis for a non-volatile memory cell.

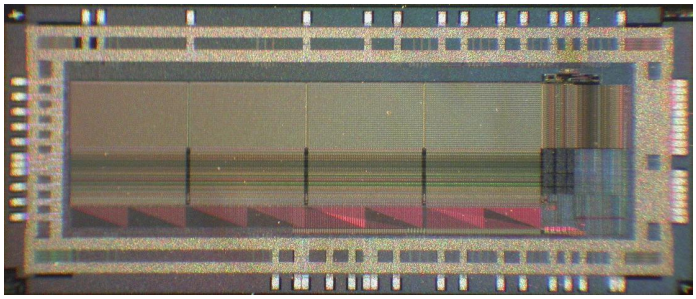
During the course of the program three cycles of design and fabrication have been completed. The first was focused on development and characterization of single-poly floating-gate memory cells (see Figure 2). EEPROM operation is based upon shifting the threshold voltage of floating-gate transistors by adding or removing charge by Fowler-Nordheim tunnelling. The threshold shift is read by turning on the floating gate device by capacitive coupling and detecting the difference in current resulting from a positively versus negatively shifted transistor threshold. Memory cell structures selected for further development were tested for data retention at 250°C for over 11,000 hours.



- **Charge is added or removed from the floating gate by Fowler-Nordheim tunneling through the tunneling capacitor oxide (voltage applied to terminals "T" and "C"**
- **Net effect is an apparent threshold voltage shift in the EEPROM transistor**
- **Memory cell is read by turning on the EEPROM transistor by capacitive coupling using the Control Capacitor**
- **Drain current is sensed to detect the difference between a "programmed" cell (stored 1) and an "erased" cell (stored 0)**

FIGURE 2: Single-poly Floating Gate Memory Cell

After the first round of silicon (focused on memory cell development), a second round of silicon was dedicated to a test-chip that focussed on arraying cells into a typical product configuration and validating means for accessing individual cells within the array for reading and writing. The demonstration vehicle was a 32Kbit memory array accessible as a 4K by 8 bit memory. This incorporated high-voltage row/column interface circuitry required for memory cell writing. High-voltage generation and waveform shaping for memory cell program/erase were generated off-chip. This demonstration memory (Figure 3) was used to verify capability for reading and writing over the full temperature range as well as further testing of data retention and data cycling in the array.



- **Off-chip program/erase waveform generation**
- **Demonstrated read/write at 250°C**
- **Data retention testing >500hrs @250°C**
- **Memory array program/erase to 100K cycles**

FIGURE 3: 32Kbit Demonstration Memory Array

Based on results from these first two test chips, a 32K x 8 HTEEPROM product design has been designed and fabricated. By means of a configuration input pin, this memory can be configured for either parallel or serial interface. The parallel interface incorporates the functionality of industry standard 28C256 parallel memories (see Figure 4). In addition it adds six I/O that are dedicated for use with the High-Temperature FPGA (these are identified by the blue font in the table embedded in Figure 4). These I/O enable the HTEEPROM to serve as a non-volatile programming device (i.e., configuration memory) for the High Temperature FPGA, capable of autonomously configuring the FPGA on power-up. The HTEEPROM also adds pins for connection to external capacitors that are required for the charge pumps that generate the high-voltage (plus/minus 8.25V) supplies needed to write the HTEEPROM.

Pin Name	Description
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
FPOR	**FPGA Power On Reset**
CCLK	**Configuration Clock**
ERR	**Configuration error flag**
CON	**Configuration Handshake**
DEFCON	**Enable FPGA SRAM Check**
CHECK	**Start SRAM Check Cycle**
A0-A14	Address Inputs
D0-D7	Data Inputs/Outputs

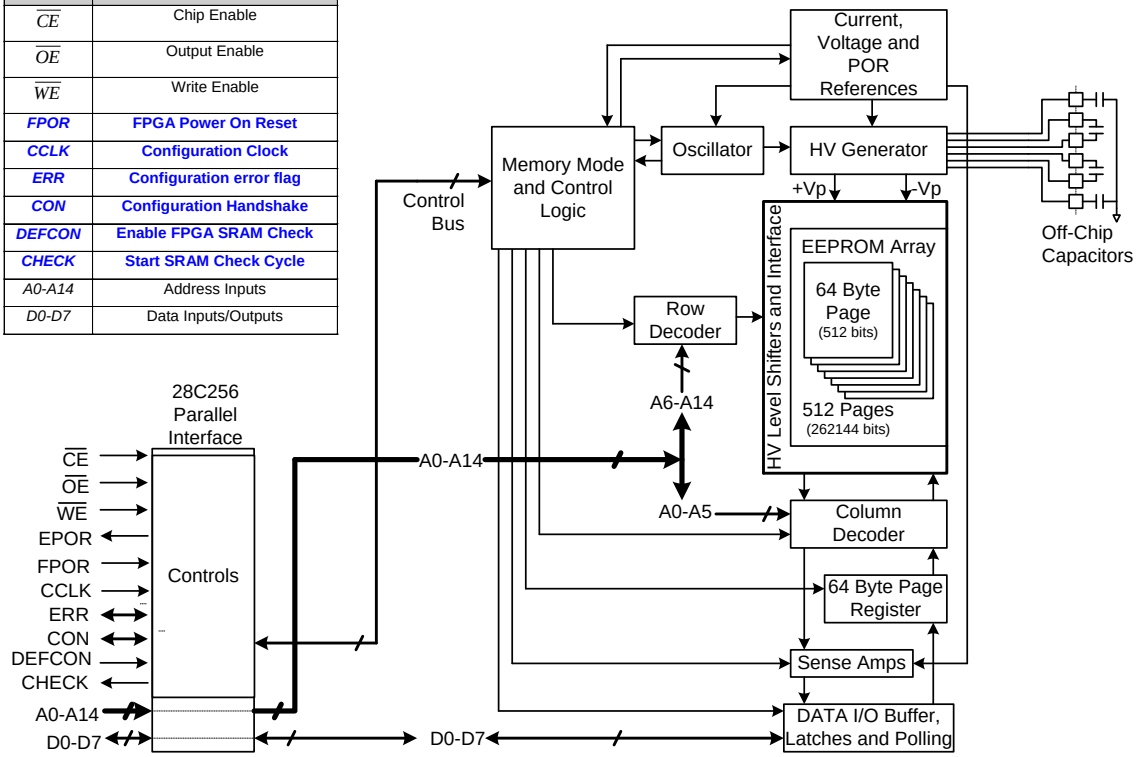
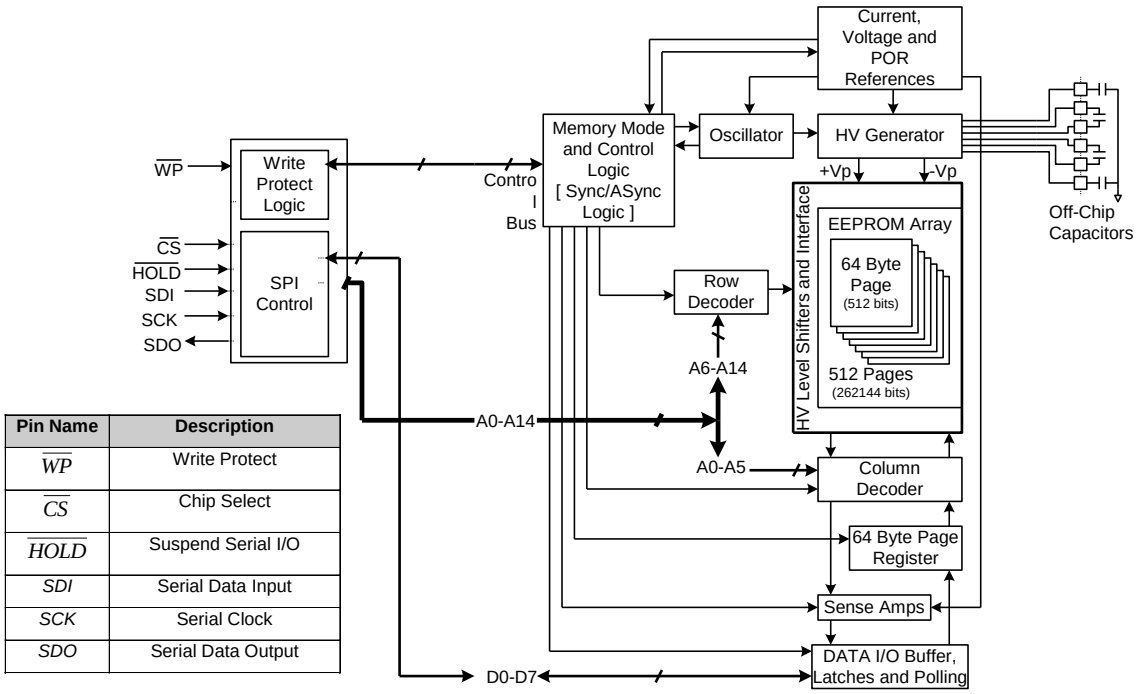


FIGURE 4: HTEEPROM Parallel Interface Configuration
(Signals listed in blue font are used for High-temperature FPGA configuration)

The serial interface configuration is shown in Figure 5. Comparison to figure 4 shows that the core functionality is not changed between the two approaches. A small amount of logic is added to the core to implement the serial interfaced control shown in Figure 5. The serial configuration incorporates the functionality of industry standard 25C256 memory devices.



Pin Name	Description
$\overline{WP}$	Write Protect
$\overline{CS}$	Chip Select
$\overline{HOLD}$	Suspend Serial I/O
SDI	Serial Data Input
SCK	Serial Clock
SDO	Serial Data Output

FIGURE 5: HTEEPROM Serial Interface Configuration

The complete 32K x 8 HTEEPROM product design has recently completed fabrication. Design verification testing will be completed during the second half of 2007. It is expected that this design will be commercialized in the form of deliverable die as well as in packages. Package development has yet to be completed.

High-temperature Multi-chip Module / RPDA Project

Honeywell was awarded a second Deep Trek project in 2006 that focuses on packaging aspects of high-temperature electronics. This new project is entitled Re-configurable Processor for Data Acquisition (or RPDA). The objective is to develop a rugged co-fired ceramic multi-chip module suitable for down-hole oil and gas exploration and/or down-hole permanent installation applications. The RDPA package will house the Deep Trek High-temperature FPGA, the HTEEPROM, and a previously developed high-temperature SOI 32K by 8 bit SRAM (HT6256). The floor-plan of the top-view looking into the RPDA package is shown in Figure 6. The underside of this package is populated with 147 pins arranged as a 7 by 21 grid on 0.1 inch spacing. In addition to the FPGA, EEPROM and SRAM, the package also will house ceramic chip capacitors required for the EEPROM charge pumps as well as power-supply transient by-pass capacitors. These capacitors, as well as all other components and materials will be capable for use at 225°C or higher.

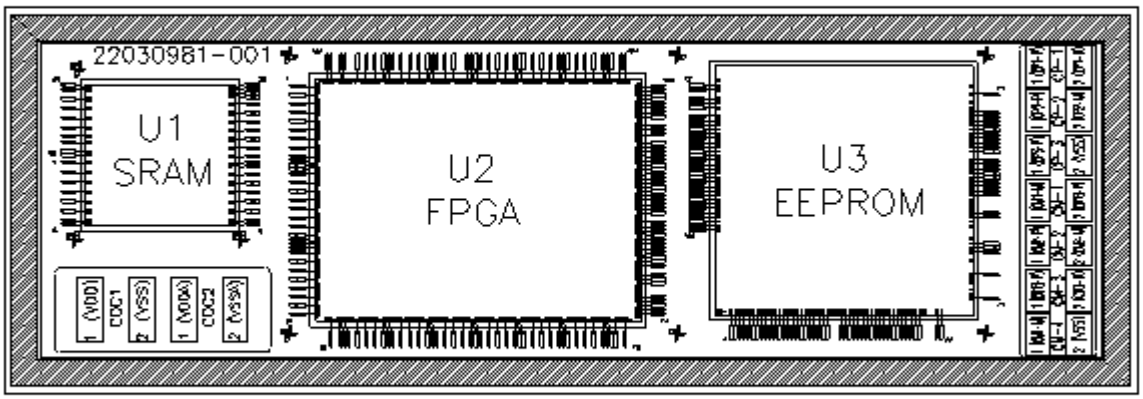


FIGURE 6: RPDA Package Component Floorplan, Top View.
Overall dimensions are 5.558 cm by 1.905cm

The RPDA package will have multiple layers of embedded interconnect. The inter-connect and I/O assignment are designed so that comprehensive testing of the individual IC's can be performed after all components have been assembled in the package. The FPGA and EEPROM interconnect will facilitate configuration of the FPGA by multiple modes, including autonomous configuration of the FPGA using data that can be pre-loaded into the EEPROM. The package will provide 55 fully configurable I/O which the user can define according to the FPGA configuration. An additional 57 I/O will have direct access to the SRAM and/or EEPROM, but can also be configured by the user. At this writing the MCM package is in the final design phase, and fabrication is planned for completion in early 2008.

In addition to the package development, the RPDA program also is chartered to develop and demonstrate configuration of the RPDA for a data acquisition function. At this time the planned configuration targets using the RPDA module to control and capture data from an external HTADC18 A-to-D converter under sampling schedules that may be established remotely via a master SPI control device. By the completion of the program in the first half of 2008 the RPDA package will be developed, fully assembled, and demonstrated in both an un-configured state as well as configured for the targeted data acquisition functional demonstration.

Summary

U.S. government and industry collaborative research under the Deep Trek programs have resulted in the successful development of SOI technology and design infrastructure for applications up to 250°C, including a family of high-temperature mask-programmable gate arrays. These have been utilized for the development, prototyping, and high-temperature functional and parametric validation of multiple components. These components, important for the realization of practical down-hole electronic systems, include high temperature versions of a dual precision amplifier, two complete A-to-D converters, and a field-programmable gate array. In addition, technical feasibility has been

established for high-temperature non-volatile memory in the HTSOI process, and this has resulted in the design and fabrication of a complete 32K by 8 HTEEPROM that is currently in design verification. Additional development under the Deep Trek program will result in a rugged package suitable for down-hole applications to house multiple components in order to develop a flexible Reconfigurable Processor for Data Acquisition (RPDA). All of these items, including design tools, wafer foundry access, and components are planned to be accessible by commercial channels within six to twelve months.

Acknowledgements

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The authors would also like to thank the member companies of the Deep Trek High Temperature Electronics Joint Industrial Participation (JIP) consortium for financial and technical support. JIP members have been: BP, Baker Hughes, Goodrich Aerospace, Halliburton (through 2005), Honeywell, IntelliServ, Quartzdyne, and Schlumberger.

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HiTEC 2008 Paper
Session WA1-1

"General Purpose 256KBit Non-volatile Memory for Operation to 250℃"

APPENDIX to
Final Report

Deep Trek
Re-configurable Processor for Data Acquisition (RPDA)

Honeywell

General Purpose 256KBit Non-volatile Memory for Operation to 250°C

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Abstract

High-temperature non-volatile memory is needed for applications such as program memory storage for micro-controllers, high-temperature data-logging, storage of calibration coefficients for sensor compensation, etc. SOI CMOS has been proposed and demonstrated as a technology suitable for implementation of high-temperature EEPROM. However, there are presently no readily available non-volatile memory components suitable for general-purpose use above 200℃. This paper describes a high-temperature general-purpose EEPROM that has been developed for use at temperatures up to 250℃. The EEPROM is implemented in high temperature 0.8 micron SOI CMOS process, with no additional steps required for non-volatile memory capability. It employs a single-poly floating-gate memory cell that can be programmed and erased over the full operating temperature range. High-voltages for program/erase waveforms are routed to the memory elements using extended-drain transistors with elevated drain/source breakdown voltage. Previous papers have described demonstration memory in this process flow that required externally-generated program/erase waveforms. This paper describes a full-featured memory design where program/erase waveforms are generated on-chip. External capacitors are used in conjunction with charge-pumps to provide high-voltage supplies for the program/erase waveforms. The HTEEPROM is 256Kbits and may be electrically configured by an input pin as either a serial or parallel memory. The design incorporates an on-chip timer to support periodic memory refresh to extend data retention indefinitely. This design is the largest high-temperature non-volatile memory to date developed specifically for high-temperature applications.

Key words: High-temperature electronics, EEPROM, Non-volatile Memory

1.0 Introduction

In extended temperature range electronic systems there is a need for non-volatile memory. In particular re-writable EEPROM memory is needed in order to store program code for microprocessors; to configure SRAM-based Field-programmable gate arrays; to store calibration coefficients, hardware ID codes, and other application-specific parameters; and to log data. Conventional non-volatile memories generally are not specified for operation above 150°C. Limitations of conventional bulk-CMOS design platforms make it difficult to extend the operating temperature of these devices beyond about 170°C. Using design methodology optimized for high-temperature, bulk-CMOS EEPROM technology has been demonstrated for 180°C application, and tested at up to 200°C [1]. Stand-alone and embedded EEPROM devices using Silicon-on-Insulator (SOI) processes have been reported [2, 3] with operation up to 250°C. However, none of these have become commercially available.

The objective of this effort is to develop a 256Kbit general-purpose High-Temperature EEPROM (HTEEPROM) capable for operation at 250°C, and that is suitable for fabrication in a commercial SOI CMOS process. General-purpose in this case means a memory device that may be configured for either serial or parallel read/write access. In addition the HTEEPROM is intended to support configuration of an SRAM-based high-temperature FPGA that was developed concurrently. In pursuing this goal, the intent is not to develop or rely on new wafer-process technology, but rather to develop the memory within the constraints of an existing wafer-process. This strategy expedites commercial product introduction .

This work has been completed with the support of the U.S. Department of Energy, under Award No. DE-FC26-03NT41834. Industrial partners in this development were Baker Hughes, BP America, Goodrich Aerospace, Honeywell, Intelliserv, Quartzdyne, and Schlumberger. However, any opinions, findings, conclusions, or recommendations expressed herein are those of the authors and do not necessarily reflect the views of the DOE or any of the industrial partners.

2.0 SOI Technology and Bit Cell Structure

As already noted, the HTEEPROM design is constrained by the IC fabrication process. The process flow in this case is a 5V partially depleted SOI CMOS process (see Table 1) that was developed specifically for high-temperature applications [4]. The relatively high threshold voltage is a result of implant adjustment so that the degradation in sub-threshold leakage current at high temperature does not affect the transistor "off current". The transistor off current (Vgs=0) at high temperature is purely a result of junction leakage rather than sub-threshold conduction.

Table 1: HTSOI Process Features

Process Feature	Typical Characteristic
Gate Oxide thickness	150 angstroms
Transistor length	0.8 microns (min.)
Target Vtn/Vtp 25°C 250°C	 1.2V / -1.3V 0.85V / - 1.0V
Sub-Vtslope, mV/dec 25°C 250°C	NMOS PMOS 150 180 260 320
Transistor "Off current" Nch, 250°C Pch, 250°C	 0.8 nA/micron width 0.5 nA/micron width

As in the previously cited SOI EEPROM implementations, there is only a single polysilicon layer in this process. Therefore, the memory element for the HTEEPROM is a single-poly floating-gate bit cell (Figure 1). The control capacitor is sized much larger than either the tunnelling capacitor or the floating-gate EEPROM transistor. Therefore, when voltage is applied across terminals T and C, it appears mostly across the tunnelling capacitor. By controlling this voltage, charge may be added or removed from the floating gate by Fowler-Nordheim tunnelling across the tunnel capacitor oxide.

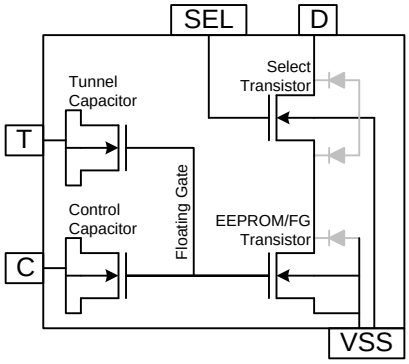

Figure 1: Floating Gate Memory Element

To add electrons to the floating gate, a positive voltage, VP, is applied to terminal C and a negative voltage, VM, is applied to terminal T, thereby driving electrons through the tunnel capacitor oxide onto the floating gate. To remove electrons from the floating gate the polarity of the voltages applied on terminals C and T is reversed.

During reading operations, terminal T is connected to VSS, and a "read" voltage of about 2.2V is applied to terminal C. The select terminal is connected to 5V, allowing the drain current of the EEPROM floating gate transistor to flow through the select transistor. The prior write operation effectively shifts the threshold voltage (Vt) of the EEPROM floating gate transistor by virtue of the charge stored on the floating gate. A sense amplifier detects the difference between the drain current and that of a replica bit cell (one without a floating gate). The polarity of the Vt shift of the EERPOM transistor determines whether the bit is detected as logic 1 ("programmed" cell) or logic 0 ("erased" cell). Note that no special oxides or fabrication modifications are employed in this approach. The capacitors within the bit-cell are MOSFET structures, although their layout geometry is not typical of a standard N-channel MOSFET.

3.0 High-temperature Device Characteristics and Considerations

Tunnelling characteristics for the N-channel Tunnelling capacitor can be seen in Figure 2. This data is obtained from a test structure with 4800 capacitors connected in parallel. Below about 9V to 11V the current follows a leakage characteristic. This leakage current does not vary between 25°C and 125°C, but is significantly elevated at 250°C. Dealing with this elevated leakage at extreme temperature is one of the challenges for meeting 250°C data-retention requirements (the ability to store logic state for

extended periods). The elevated leakage current at 250°C reduces the length of time that charge can be reliably stored on the floating gate of the bit cell. In general it will be necessary to refresh (i.e., re-write) the data to the bit cell at intervals in the range 500 to 1000 hours if the memory is continuously operating at 250°C. Even at 250°C data retention can be significantly enhanced if the bias across the tunnelling oxide is 0V. Indeed, the bit cell of this memory was characterized on test structures for data retention [5]. In this test, the device was un-powered between test readings and it was observed that for an un-disturbed bit cell sufficient charge was stored on the floating gate to enable reliable reading after 10,000 hours at 250°C.

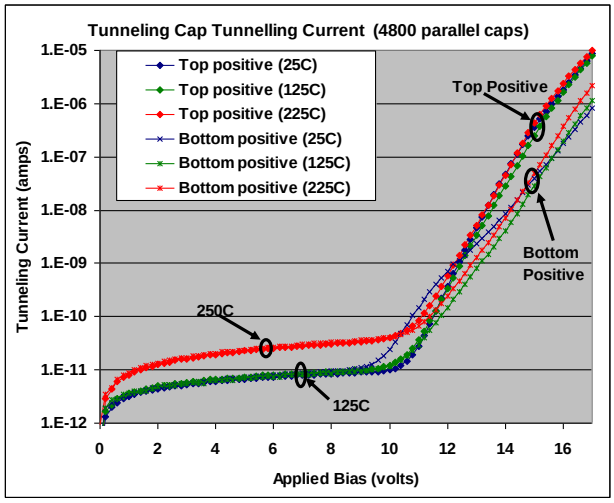

Figure 2: Tunnelling Current vs. Temperature and Voltage

Tunnelling current begins between 9V and 11V. At higher voltages (above 14V) there is not a large difference in tunnelling current characteristics with temperature. However, there is a significant difference in the magnitude of current based on polarity of the applied bias. For this reason, the time that a voltage must be applied to transfer electrons onto the floating gate (reducing the apparent Vt) is significantly less than the time required to remove that same amount of charge. This leads to design considerations for the duration of high-voltage waveforms generated to write the memory.

Another challenge for HTEEPROM implementation is the requirement for the generation and routing of high-voltages, in excess of the 5V operating range normally employed for this technology. To generate and route these voltages extended-drain MOSFET devices (referred to at lateral DMOS) are used. The drain terminal is pulled away from the gate of the device and extended to the gate via the well-implant normally used for the opposite device type. For example, an N-channel DMOS device is fabricated with a P-well under the gate and the N-well implant (normally used for P-channel devices) is used between the gate edge and the drain terminal. This approach does not require any additional process steps.

Minimum dimension DMOS devices are used in level-shifters and as switches in the memory row and column interfaces. "ON" and "OFF" characteristics for minimum geometry layouts are shown in Figure 3. These curves show that the drain voltage can extend to 20V and that even at 250°C the ratio of on/off current spans four orders of magnitude.

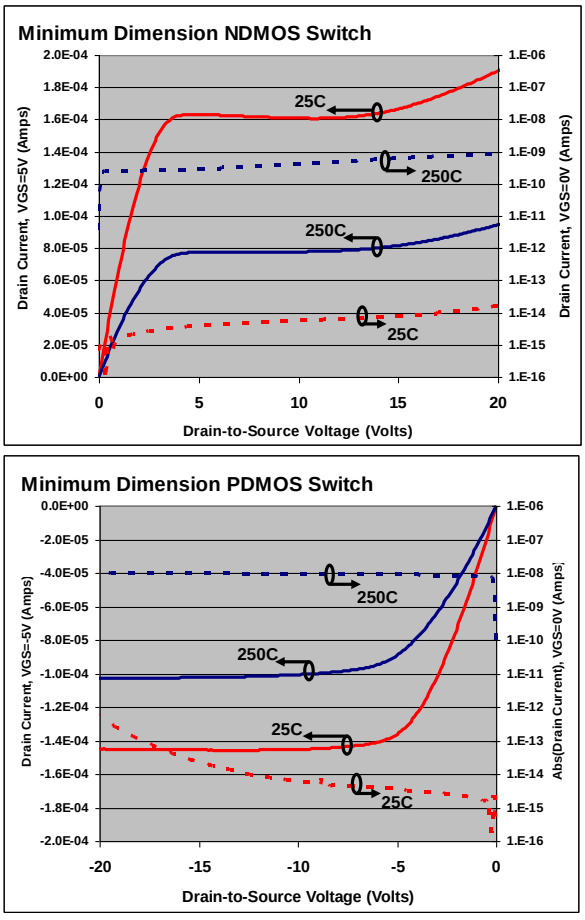

Figure 3: N-channel and P-channel extended-drain lateral DMOS "ON" Current and "Off" Leakage (Leakage normalized to minimum width)

4.0 High-temperature EEPROM Functional Approach and Demonstration

Write waveforms used to write data to the bit cell are shown in Figure 4. The SOI technology has been used to advantage in that it is practical to generate both positive and negative voltages (via charge pumps) on the chip without having to consider substrate biasing (since all of the active devices are oxide isolated). On-chip charge pumps have been designed so that when writing is performed a positive voltage (VP) and a negative voltage (VM) are generated, each with amplitude of approximately 8.5V. Voltage amplitude is set in proportion to an on-chip band-gap voltage reference that uses PMOS structures configured as lateral PNP bipolar transistors. Off-chip capacitors are used to support the multi-stage charge pump operation.

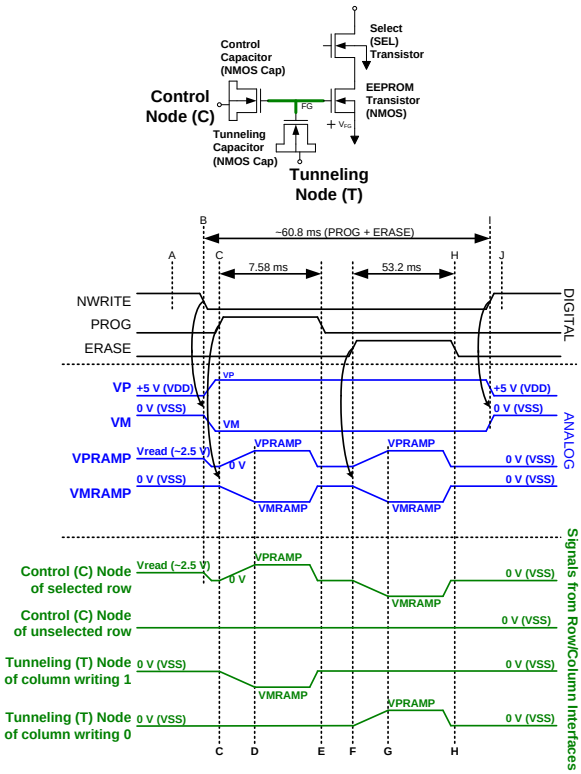

Figure 4: HTEEPROM Write Waveforms

During writing, waveforms VPRAMP and VMRAMP are developed and routed to the memory array according to the scheme of Figure 4. The Control node of unselected rows remains at 0V through the writing process. The Control node of selected rows is connected first to the positive ramp voltage (VPRAMP) and then later to the negative ramp voltage (VMRAMP). In selected columns the Tunnelling node is also alternately connected to VMRAMP and VPRAMP as shown in Figure 4.

This approach enables the generation and routing of voltage through most of the array that, at 8.5V or less, are below the tunnelling voltage and therefore do not significantly disturb cells that are not being written. For cells that are being written, voltages are applied across the tunnelling capacitor that are approximately 14.5V (after accounting for voltage reduction according to the capacitance ratios of the Control vs. the Tunnelling capacitor and floating gate transistor). This voltage is sufficient for tunnelling. Note that the dwell times of the write waveforms are controlled so that writing a "0" (positively shifting the Vt of the floating gate transistor) is given 7x the dwell time as writing a "1" (negatively shifting the Vt of the floating gate transistor). The total duration of each write operation is approximately 60 milliseconds.

The amplitude and dwell time of these waveforms were established and characterized using a 32Kbit (4K x 8) demonstration memory (Figure 5). This device contained a complete 512 x 64 array of memory cells with row/column decoding and high-voltage interfaces. Write waveforms and control signals were generated off-chip for this demonstration. This chip allowed for data retention testing, as well as memory cycling (durability testing) and testing of the read-out circuitry (sense amps and references).

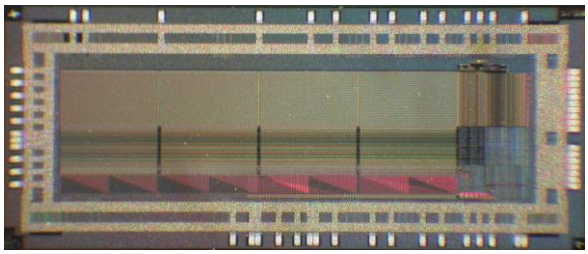

FIGURE 5: 32Kbit (4K by 8) Demonstration Memory

It is well known that floating gate memory devices that employ Fowler-Nordheim or hot-electron tunnelling exhibit degraded write capability with the accumulation of program/erase cycling. This is observed as a diminished capability for charge transfer through the tunnelling oxide. This limits the number of cycles that can be applied to a given bit-cell consistent with reliable data storage.

In developing a high-temperature EEPROM, it is necessary to consider the additive combined effect on read-out from both data cycling (durability) as well as charge leakage (data

retention) at 250°C. Data retention can also be impacted by the bias conditions during the idle state. As noted in the discussion of tunnelling current (see Figure 2) a powered idle condition with voltage applied across the tunnelling capacitor results in leakage that is elevated relative to an zero-bias or un-powered state. The question of bias during an idle state is relevant to the access time of the memory. For lowest read-access time it would be preferred that the read voltage (approximately 2.2V) be applied to the Control nodes of all of the rows of the memory array while it is in an idle state (rather than waiting to charge and settle the read voltage on an address change). In other words, there is a trade-off between read-access time and powered data retention at high-temperature.

Figure 6 summarizes the combined effect of 250°C data retention and the number of program/erase cycles. Memory cells were written a total of 100,000 times (alternating 1 and 0) using a total voltage for writing of 16.5V (plus/minus 8.25V applied across the Control and Tunnelling nodes). Dwell times were set to give a symmetric Vt shift that was initially plus/minus 1.35V (for writing 0/1 respectively). It can be seen that after 3 weeks at 250°C there is still significant Vt shift (>1.2V, or plus/minus 600mV) that can be reliably sensed through the read-out circuitry. Separate testing under power with/without read-bias voltage applied to the Control node resulted in an additional 150mV to 200mV of Vt-shift lost when the read-bias voltage is continuously applied to the control node. Other rows of these same devices were cycled 1 million times and successfully read after 537 hours at 250°C (un-powered data retention testing).

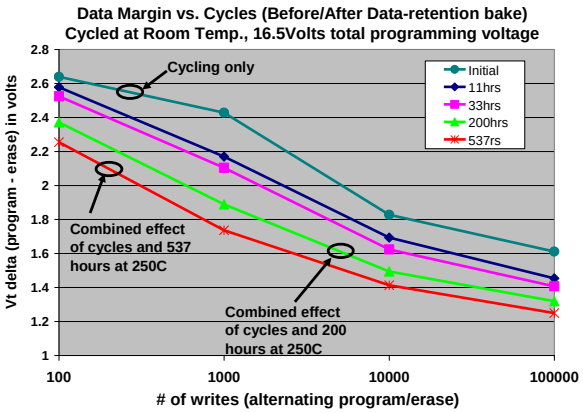

FIGURE 6: Data Retention and Data Cycling Results from 32Kbit Demonstration Memory

The demonstration memory also includes test modes where the entire memory can be addressed simultaneously for cycling tests of the bit cells. Entire arrays of the 32Kbit memory were cycled (alternately writing 1's and 0's) for 100,000 cycles without any bit-errors detected. Note that these cycling tests were performed at room temperature.

Time-dependent dielectric breakdown (TDDB) is an additional consideration for the HTEEPROM development. The HTEEPROM employs a CMOS SOI process with 150 angstrom gate oxide that is used primarily for 5V applications. During the write process large areas of gate oxide within the HTEEPROM are stressed with voltages in excess of 5V. This is in addition to the bit cells being written (for example, all of the tunnelling capacitors in cells that are not being written). For the final 256Kbit HTEEPROM design, each write operation involves stressing approximately 418,000 square microns of gate oxide at 8.5V for up to 60msec.

Large area gate-oxide test structures were tested for time-dependent breakdown as a function of applied voltage at 125°C and 250°C. Results are summarized in Figure 7. Extrapolating from the accelerated test conditions to 8.5V predicts over 2000 hours at 8.5V. This time is equivalent to the cumulative stress of 120 million write operations. Note that the area of the oxide stressed in these tests represents approximately 40% of the total area that would be stressed during a write operation of the 256Kbit EEPROM. These results are preliminary, and were intended to establish the bias conditions for subsequent 250°C testing with a larger sample size, and at bias conditions closer to actual use conditions. This additional testing is in progress at the time of this writing.

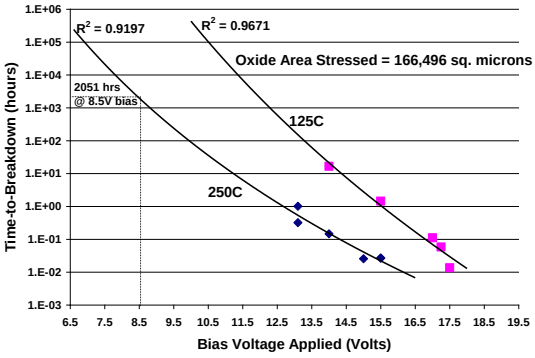

Figure 7: Gate-oxide time dependent breakdown for 166,496 square micron gate oxide test structures

5.0 HTEEPROM Product Configuration

A complete 32K x 8 HTEEPROM product configuration has been designed and fabricated in accordance with the technology concepts, bit cell structure and operating principles already discussed. An overview of the product architecture and I/O signals is shown in Figure 8. The memory array includes 512 columns of data storage elements plus an additional 56 columns used for Error-Correction Coding (ECC). The ECC corrects for single-bit errors within a page, where a page consists of 64 bytes within a given row (1 byte = 8 bits). A digital logic block provides parallel mode access where the memory may be addressed and asynchronously read as a 32K by 8-bit memory. Worst-case parallel mode access times at high-temperature are expected to be 150nsec. The parallel interface incorporates the functionality of industry standard 28C256 parallel memories, including page buffer and control sequencing for both page-mode and byte-mode writing schemes.

All of the reference and bias voltages, timers, and write-control circuitry is included on-chip, with the exception of charge-pump capacitors. These are off-chip in order to preserve die area and ensure sufficient charge storage to operate in the presence of leakage current at 250°C.

A memory-refresh strategy is employed to enable long-term data storage at 250°C. A memory refresh-request pin goes high on power-up and approximately every 30 days thereafter to request memory refresh. If this signal is acknowledged via a refresh-acknowledge input then the memory will re-write itself in 512 sequential page-write operations. The refresh requires approximately 31 seconds to be completed. Note that this refresh is optional and may be ignored by the system. The initial power-on refresh requests "expires" after approximately 20 seconds if it is not acknowledged. In addition, due to the page-mode writing scheme, writing to any byte within a page effectively refreshes the entire page.

The parallel mode configuration includes six I/O that are dedicated for use with the High-Temperature FPGA. These I/O serve as control signals enabling the HTEEPROM to be used to load and verify configuration for a high-temperature FPGA that was developed concurrently with the HTEEPROM. Configuration of the FPGA can require up to half of the HTEEPROM capacity. Once the configuration is complete the device reverts to the standard parallel-mode operation and the remaining HTEEPROM capacity may be used by the system for other purposes. A configuration-protect pin provides for hardware write-protection of the lower half of the HTEEPROM address space, which would be that portion normally used for FPGA configuration.

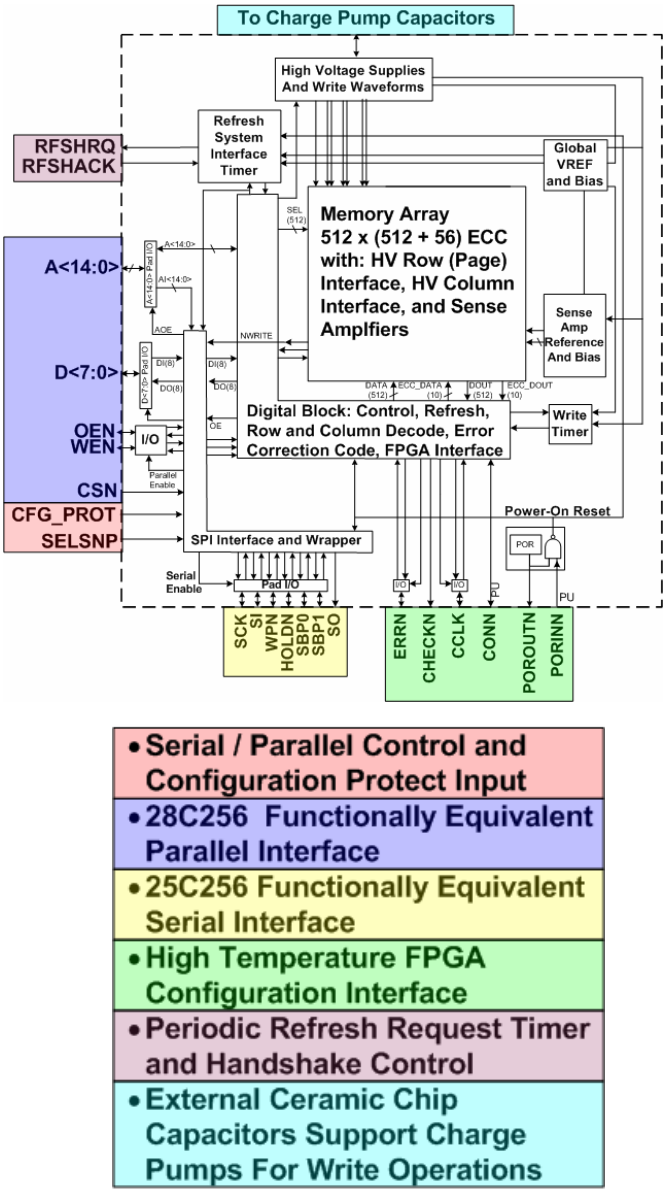

FIGURE 8: HTEEPROM Architecture and Top-level Interfaces

Serial-mode operation can be invoked by a Serial/Not-Parallel configuration pin. If this pin is pulled high, then the memory is accessible for read/write access as a serial device via SPI interface in accordance with industry standard 25C256 serial memories.

The complete 256Kbit HTEEPROM product design has recently completed fabrication. A die photo is shown in Figure 9. Verification testing is on-going. As sufficient testing is successfully completed the intention is to develop commercial product specifications that support 250°C operation, production test development, and package development. It is expected that this design will be commercialized in the form of deliverable die as well as in hermetically sealed ceramic packages suitable for 250°C.

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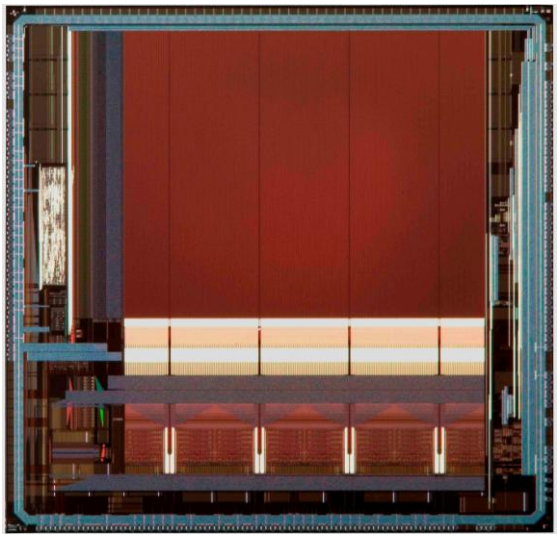

FIGURE 9: HTEEPROM Die Photo
Die Size is 12.3mm x 12.7mm

6.0 Summary and Conclusions

A commercial high-temperature SOI CMOS process flow has been shown to be capable for the development of a High-temperature floating-gate non-volatile memory element, without requiring the addition of process steps or special features. This has been shown through the characterization of tunnelling current and high-voltage device capability, and by the development and data retention testing of bit-cells.

Operating principles for a complete HTEEPROM product based on the floating gate memory elements have been developed and verified by the fabrication and testing of a 32Kbit demonstration memory. This includes additional data retention and data-cycling tests at room temperature and at 250°C. Results indicate that the approach can support millions of write operations and at least 100,000 program/erase cycles for each of the individual bits within the memory.

Finally, a complete product configuration has been designed and fabricated as a 256Kbit HTEEEPROM. A data refresh scheme and Error-correction Coding are employed to ensure reliable long-term data storage and read-out at up to 250°C. The design is flexible to support both serial and parallel mode read and write operation, and incorporates an FPGA loader to automatically download configuration data into an SRAM-based FPGA. Design verification of this product configuration is a current task, to be followed by development of high-temperature packaging, screening tests, and datasheets suitable for commercial product offering.

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Session WA1-3

"Single Package Re-Configurable Processor for Data Acquisition at 250℃"

APPENDIX to
Final Report

Deep Trek
Re-configurable Processor for Data Acquisition (RPDA)

Honeywell

Single Package Re-Configurable Processor for Data Acquisition at 250°C

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Abstract

A high-temperature data processing device is required for applications gathering sensor data and control of electronics in environments which operate above 200°C. This paper discusses the process of leveraging advances in high temperature electronics and integrating them for new applications and improved system performance. It centers on the development of the 250°C High Temperature (HT) SOI CMOS process technology, several new HT products, and HT package technology. Honeywell integrates a HT FPGA, SRAM and EEPROM into a Multi-Chip Module (MCM) creating a flexible, re-configurable computing platform for sensor data processing and control applications at 250°C. A reconfigurable processor enables the ability to gather information from multiple sources and then control multiple devices with a single electronics assembly while reducing size, weight and power. Packaged in a small 2.2 x 0.75 inch (56 x 18 mm) MCM, the module operates at clock rates up to 10MHz from a single 5V supply. Although power consumption is strongly dependent on configuration, the targeted demonstration configuration clocked at 1MHz power dissipation is on the order of 100mW. The combination of all these technologies and application code to operate the module provides a significant improvement over existing technology for data acquisition applications.

1. Introduction

Due to the need for High Temperature (HT) electronics, small size and ability to survive in very rugged environments, a module integrating several key data processing components is being presented. Starting from a base high temperature SOI CMOS technology, key electronic functions are developed and then integrated. Each of these are addressed individually and then directed towards a multi-channel data logging application. The MCM design and manufacturing provide long life at high temperatures (250°C) and high reliability in extremely harsh environments.

This MCM is referred to as the Reconfigurable Processor for Data Acquisition (RPDA). Its use is illustrated in a sensor data conversion application referred to as a Multi-Channel Data Acquisition Controller (MCDAC).

2. HT SOI CMOS Technology

The Integrated Circuits (ICs) are manufactured on 0.8um Silicon On Insulator (SOI) CMOS technology. SOI CMOS has a number of features which allow for electronics to operate at temperatures at and above 250°C.

- Lower Leakage Current – The full oxide isolation SOI technology minimizes junction size and the leakage current which doubles every 10°C (above ≈170°C). The design of the transistors also re-targets transistor threshold voltage implants to reduce leakage.

- Lifetime Extension at High Temp – Electromigration increases at high temperatures and so the IC design and layout rules lower the current densities increasing reliability and lifetime.

3. Package Design and Assembly

High-reliability, high-temperature packaging is an essential element of high temperature systems. The integrated circuits are packaged in a co-fired ceramic Multi-Chip Module (MCM) which provides stable performance at temperatures greater than 250°C. The RPDA MCM has 147 pins (through-hole) to withstand high shock and vibration environments and also contains ceramic chip capacitors.

Proven materials and processes include:

- Package Type: High Temperature Co-fired Ceramic MCM
- External Metal (Plating): Gold over Nickel
- Die Attach: Adhesives and bonding materials to 300°C
- Wirebond: Aluminum
- Hermetic Seal: Welded Kovar Lid

4. Reconfigurable Processor for Data Acquisition (RPDA) Description

Three ICs are integrated into the 147 pin package to implement the RPDA.

- The HTFPGA has equivalent capacity to an Atmel AT6010 component. This provides up to 6400 register elements and/or up to 32,000 equivalent gates of logic. The number of useable gates is dependent upon the application, complexity of the signal routing, and the synthesis process (i.e., the process by which a behavioral design is translated into a gate-level structural design).
- The HTEEPROM has 256Kbits (32k x 8) of total capacity. It is intended to store configuration data that is used to program the HTFPGA and still have space available for non-volatile data storage. Internal voltages of +/-8.5V are used to write memory. The EEPROM can be accessed directly from the module pins with a parallel or serial SPI interface.

  The parallel pins are internally shared with the FPGA, so applications that require loading data into the EEPROM will need to do this while the FPGA signals are in high impedance state.
- The HT6256 SRAM has 256Kbits (32k x 8) of total capacity. The static random-access memory is asynchronous and used for application data memory.
- The small 2.2 x 0.75 inch (56 x 18 mm) HT MCM package technology is an essential element of high temperature electronic systems. Co-fired ceramic Multi-Chip Modules (MCM's) can meet this need with stable performance at temperatures greater than 250°C.

The basic interconnect diagram is shown in Figure 1. The diagram shows access to the interface of the individual ICs. This combined with the programmable I/O of the FPGA delivers the capability to expand the function of the RPDA to control additional devices, add more SRAM or EEPROM or even interface multiple RPDAs.

The proposed RPDA assembly is shown in Figure 2.

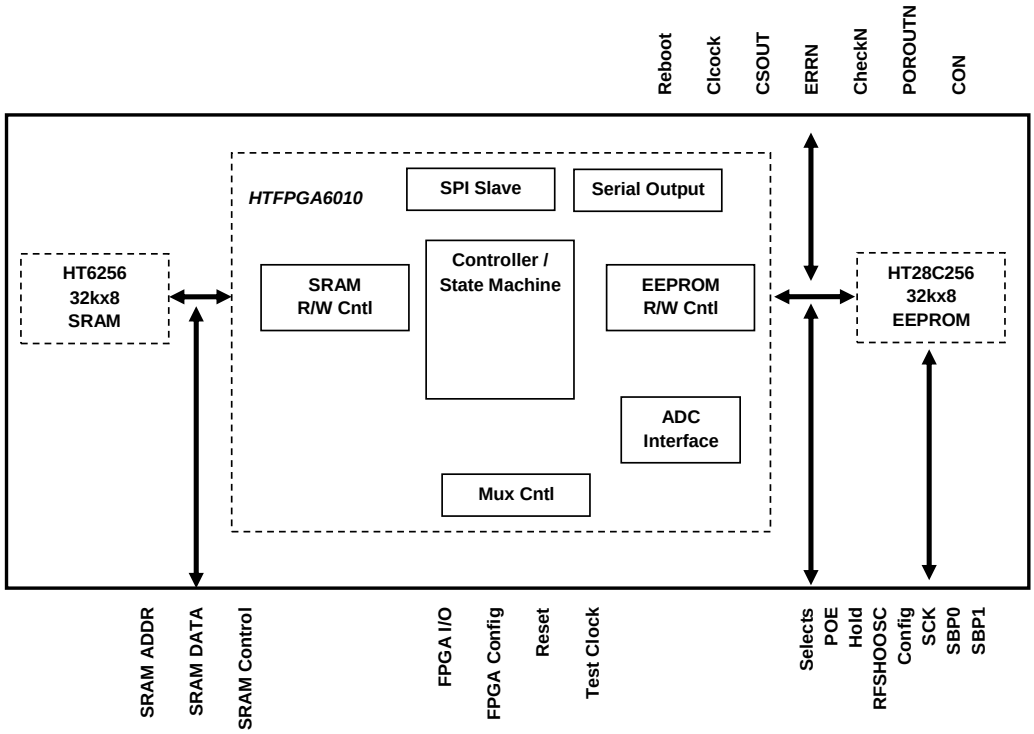


Figure 1 – RPDA Interconnect Diagram

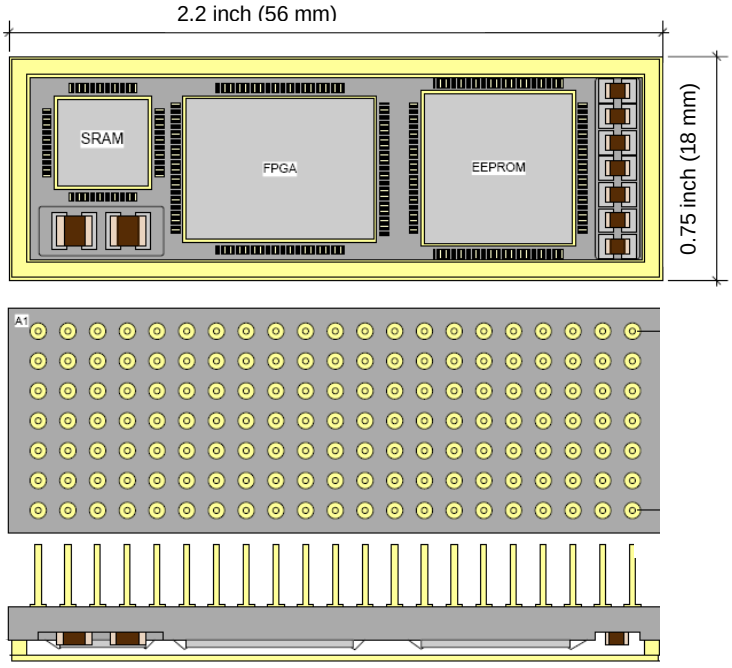


Figure 2 –Hermetic High Temperature RPDA Package, 147 Pin

The FPGA is the central controller and primary interface for data acquisition applications. With the flexibility of re-configurable logic and IO, the FPGA can be adapted to a wide variety of purposes. The RPDA has up to 115 programmable IO (54 configurable IO, 57 shared IO with direct access to SRAM/EEPROM bus) that can be configured by user.

Upon power up, the FPGA is loaded with the configuration data stored in the EEPROM. Loading the configuration data into the EEPROM can be accomplished using a dedicated serial peripheral interface (SPI) bus which is independent of the FPGA, or through the parallel bus which is common with the FPGA.

The SRAM is tightly coupled to the FPGA allowing for use as short term memory applications within the RPDA.

5. Typical Specifications

Parameter	Value
Supply Voltage	5V
Primary Clock	1 MHz
Core Data Rate	100 kHz
Sampling Period	2 sec
Data Download Rate	100 kbps
Operating Current (estimated)	20 mA
Power (Estimated)	100 mW

6. Design and Verification Tools

The RPDA MCM was designed and verified using a number of different development tools. High level simulations were performed to verify interconnect and performance of the three ICs as well as design verification of the FPGA code.

Verification simulations included:

- HTFPGA has been simulated at the logic-gate level.
  - Min/max timing parameters used in simulation
  - RPDA RTL simulations have been performed
  - Exercised HTFPGA/EEPROM and HTFPGA/SRAM interfaces
- MCDAC functional simulations have been performed
  - Exercised HTFPGA/EEPROM/SRAM using test bench
  - Simulations completed post-route HTFPGA timing files
- In addition to the gate-level structural simulations, Register-transfer-level (RTL) simulations were performed at the top-level of the RPDA to verify correct connectivity between the HTFPGA / HTEEPROM and the HTFPGA / HT6256 SRAM.

Schematic Capture and Simulation Tools

- Mentor DA en2002 – schematic capture
- QSimPro 2004SP5 - HTFPGA Quickpart Simulations
- Modelsim 5.8d – HTFPGA Quickpart Simulations
- Modelsim 6.1e – HTFPGA/RPDA HDL Simulations

Logic Synthesis and Routing Tools

- Mentor LeonardoSpectrum 2006b.12 – synthesis
- Atmel Figaro version IDS7.6.7 – P&R
  - Patch level 3 applied (RHrFPGA)
  - HT patch installed (AT6010HLV-010QM)

7. Test Plan

The RPDA test plan includes verification at several levels. The individual die are tested at the wafer level prior to the sawing process. This will include a combination of DC characteristics and functional testing. Once assembled into the MCM, further testing on the DC characteristics and higher level functional test program will take place to verify the interconnect and overall performance. Test vectors generated during the design verification will be used for the functional testing. As part of the product screening, the MCM would be burned in at a temperature of 250°C.

8. RPDA Operation and MCDAC Application

In the MCDAC application, the MCM is configured to control an eight channel analog mux and an 18-bit analog-to-digital converter. The HTEEPROM is only used as a boot ROM which contains the programming for the HTFPGA. The HTSRAM is used as data storage space in the form of an 8K by 32-bit FIFO. The MCDAC can be programmed through external pin selection to perform autonomous measurements of 1 to 8 channels of analog data on a pre-defined schedule. It may also be requested to make asynchronous reads of the ADC by providing signals to the SAMPLE NOW pin and providing a CHAN SELECT address. Control of the device and

unloading the sampled data is stored in the FIFO is through the slave serial port interface (SPI).

The FPGA will be designed to include a main Controller/State Machine. When operating autonomously, it controls the analog mux and will request data and status from the ADC. It then will place the data in memory and prepare it for transmission back to the SPI slave device. All other requests from the SPI Slave block will be handled by the Controller. A typical state diagram is shown in Figure 3.

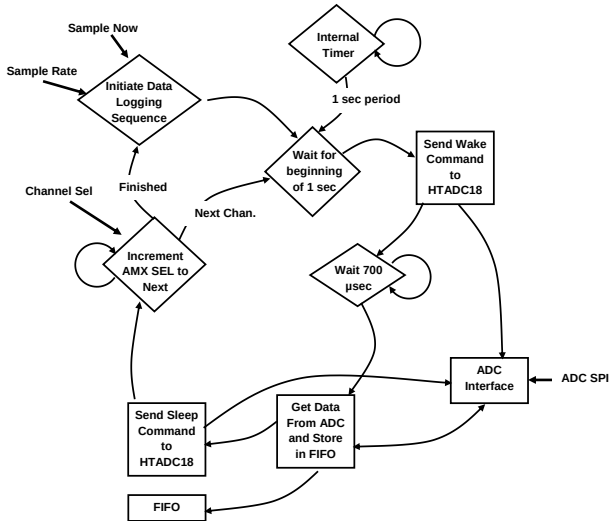
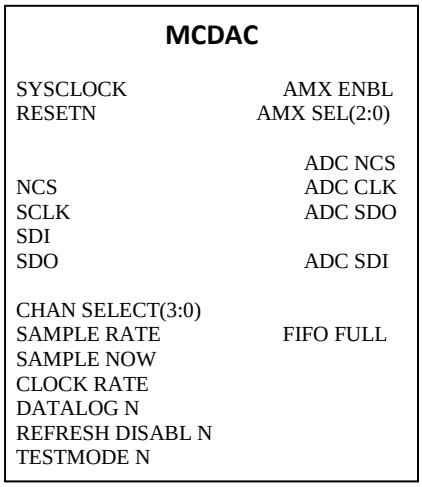


Figure 3 – Typical State Diagram

The SRAM R/W block will access the SRAM's data, address and control ports. It will provide the controller with temporary memory for storing data and status that has been collected from the ADC. Each 18-bit measurement will be stored along with health and status information into a 32-bit word. Up to 8192 32-bit words (8k x 32) can be logged by the on-chip memory. The SPI interface is used for data transfer to and from the MCDAC at data rates up to 1MHz. The SPI bus is activated through a chip select, enabling communication via the SPI Data In and SPI Data Out pins. The FIFO data can be downloaded sequentially, or most recent measurement data can be downloaded.

The functional RPDA signals used for the MCDAC application are shown Figure 4.



Signal	Type	Function
SYSCLOCK	IN	1MHz Module Clock
RESETN	IN	Global Reset
ADC_NCS	OUT	ADC SPI Chip Select
ADC_CLK	OUT	ADC SPI Clock
ADC_SDO	OUT	ADC SPI Serial Data Out
ADC_SDI	IN	ADC SPI Data In
NCS	IN	SPI Slave Chip Select
SCLK	IN	SPI Slave Clock
SDO	OUT	SPI Slave Serial Data Out
SDI	IN	SPI Slave Data In
CHANNEL_SEL(3:0)	IN	Analog Channel Select
SAMPLE_RATE(1:0)	IN	Autonomous Sample Rate
SAMPLE_NOW	IN	External Sample
DATALOG_N	IN	Enable/Disable FIFO
AMX_ENA	OUT	Analog MUX Enable
AMX_SEL(2:0)	OUT	Analog Mux Select Bus
FIFO_FULL	OUT	FIFO Full Indicator
REFRESH_DISABL_N	IN	Enbl/Disbl EEPROM
CLOCK_RATE	IN	SYSCLK Rate (1=1MHz,
TESTMODE_N	IN	Manufacturing Test Signal

Figure 4 – RPDA Symbol And Signal Definition For MCDAC Application

A functional block diagram of the MCDAC application is shown in Figure 5.

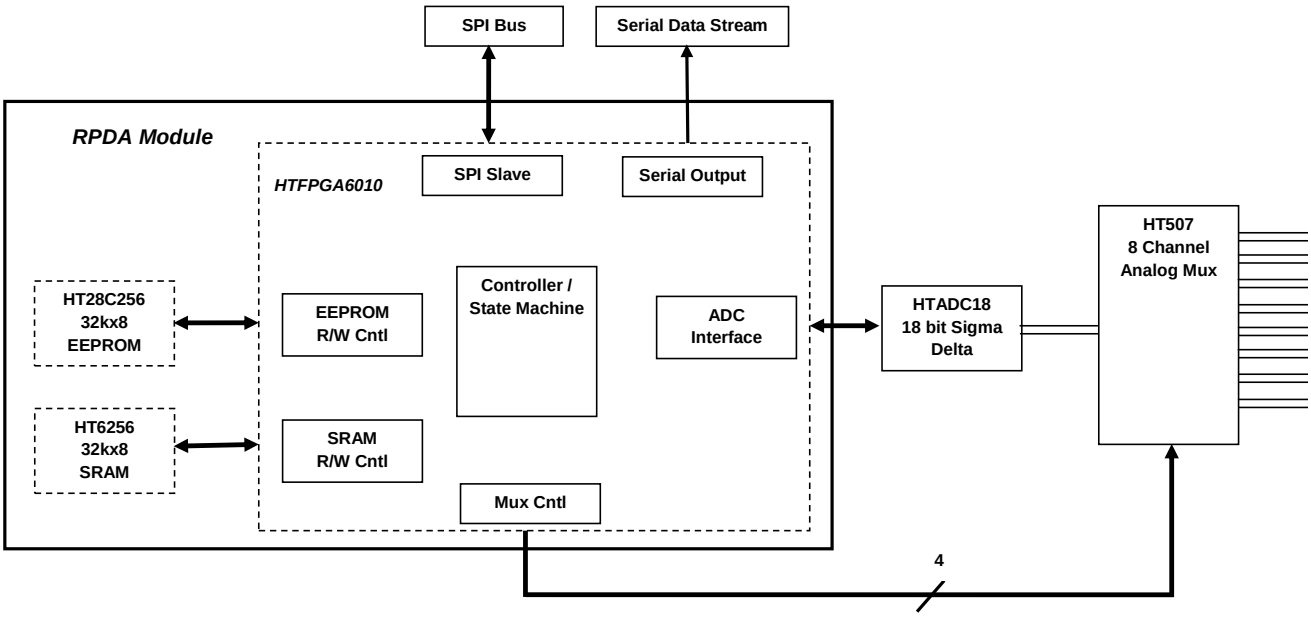


Figure 5 - Multi Channel Data Acquisition Application

9. Summary and Conclusions

In order to fulfill the need for data logging and control applications at extreme temperatures, an electronics module leveraging advances in high temperature SOI CMOS, circuit design and packaging has been defined. The combination of technologies and integration of an FPGA, EEPROM, and SRAM in the RPDA has created a flexible, re-configurable data processor. Packaged in a rugged multi-chip module provides size and power reduction allowing electronics to be installed in small spaces with temperature extremes greater than 250°C such as engines and down-hole drilling applications.

With access to the interface of the ICs, easy expansion for many applications is attained.

10. References

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