A History and Overview of the International Technology Roadmap for Semiconductors (ITRS) 2005

For the DOE Solid State Lighting (SSL)
Program Planning Workshop
Orlando, Florida – 02/02/06

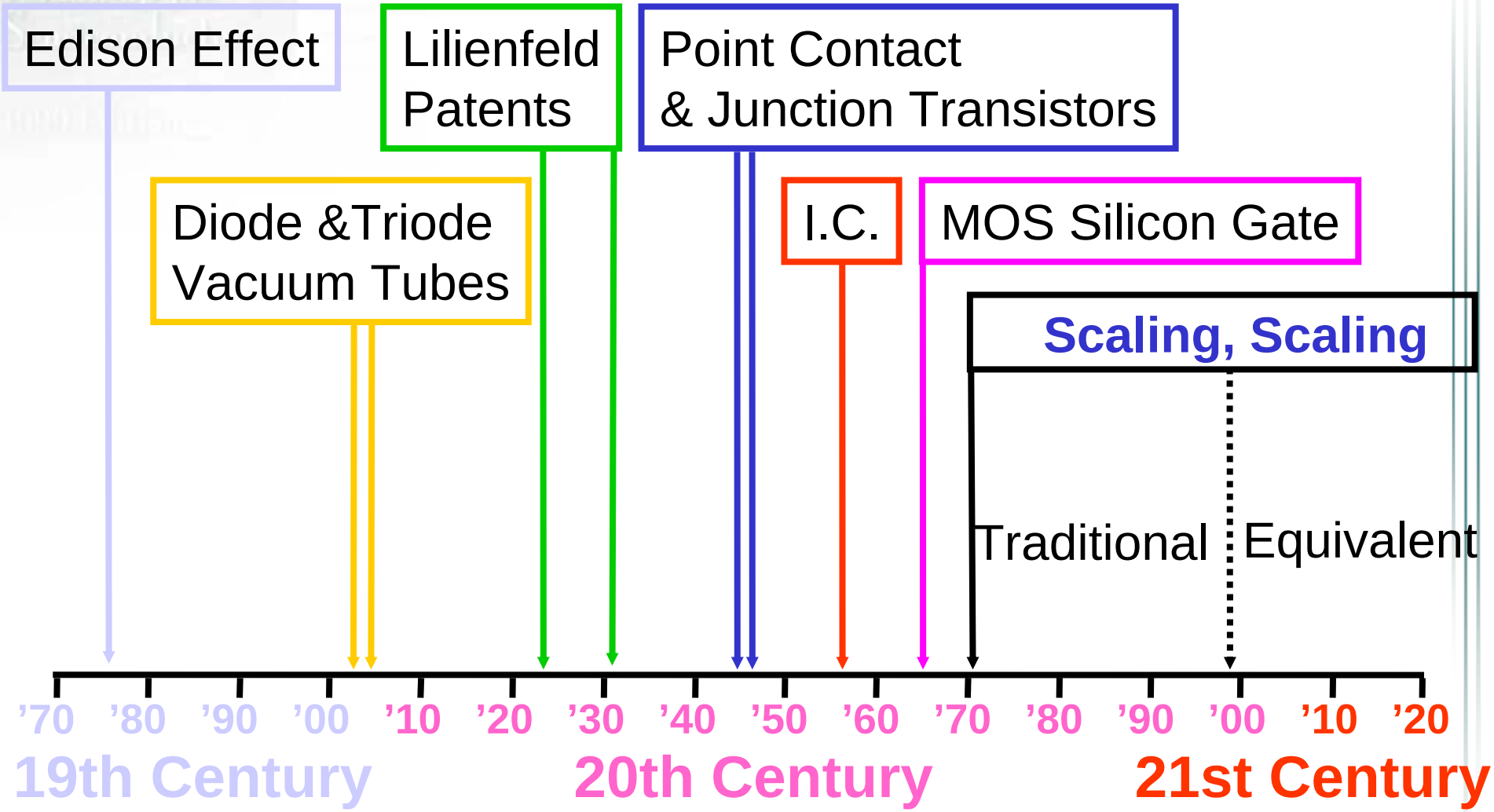
Final Draft Work – 02/01/06

2005 ITRS Overview Topics

[Summarized from History, plus Seoul Public Conference Dec'05]

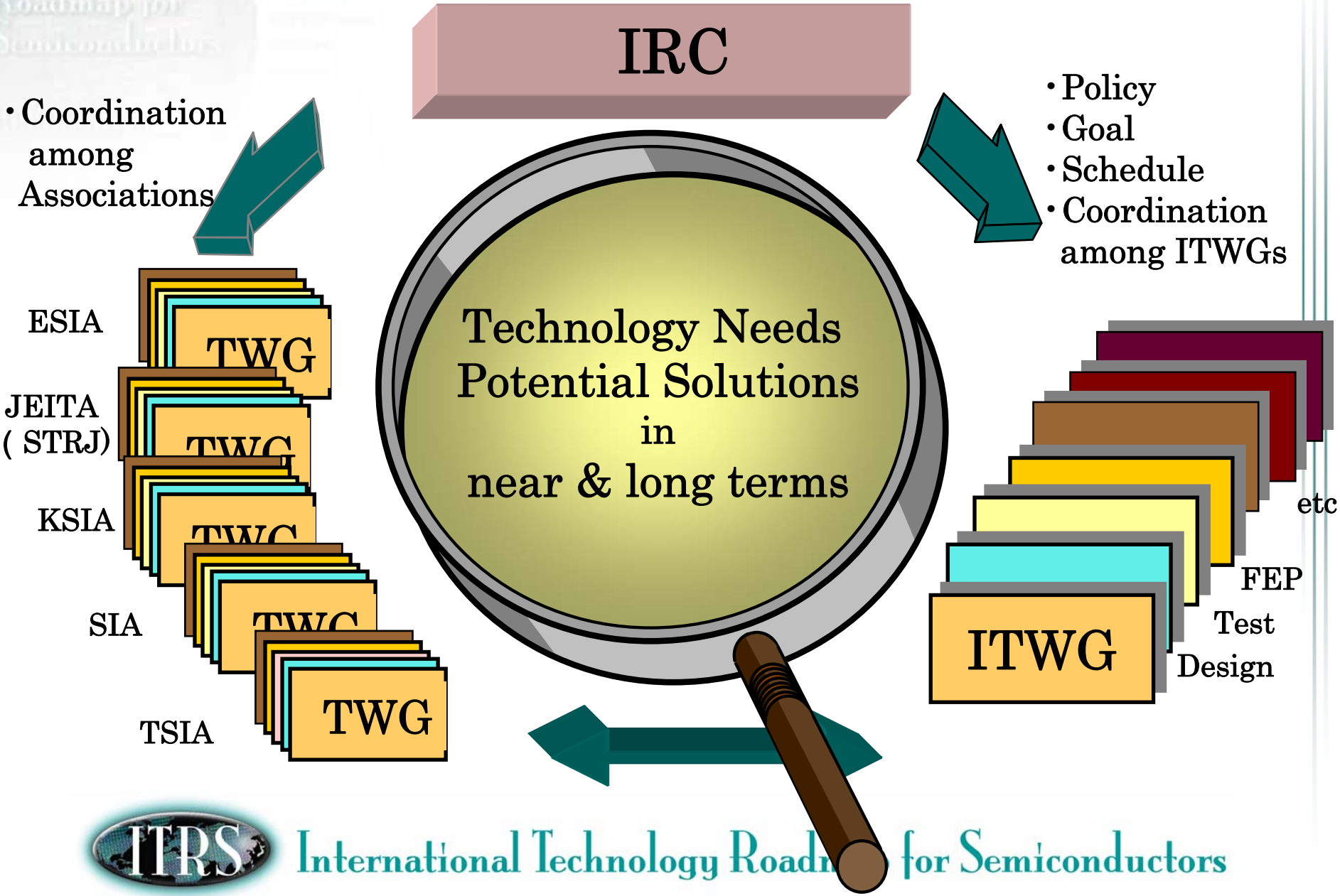
- ITRS History/Demographics
- Trends
  - More than Moore
  - 450 mm Wafer Size
- Technology Pacing
- Lithography Front End Processes/PIDS
- Interconnect
- Economic Trends
- for more information -- web sites

150 Years of Electronics



Source: Intel/P.Gargini

ITRS Mission



THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) GOALS:

• Present an **industry-wide consensus** on the "best current estimate" of our future research and development needs out to a 15-year horizon.

• Provide a **guide** to the efforts of research organizations/sponsors (industry, government, and universities.)

...Based on **premise** of continuing the four-decade-long trends of an industry that has distinguished itself by:

- rapid pace of improvement in its **products**
- exponential improvement of manufacturing capability and productivity to reduce the minimum **feature sizes**[SCALING] and **cost/function** used to fabricate integrated circuits.

From Strategy to Implementation

ITRS

Technology Needs

Potential Solutions

Consortia

Researchers

Suppliers

Detailed Solutions

Suppliers

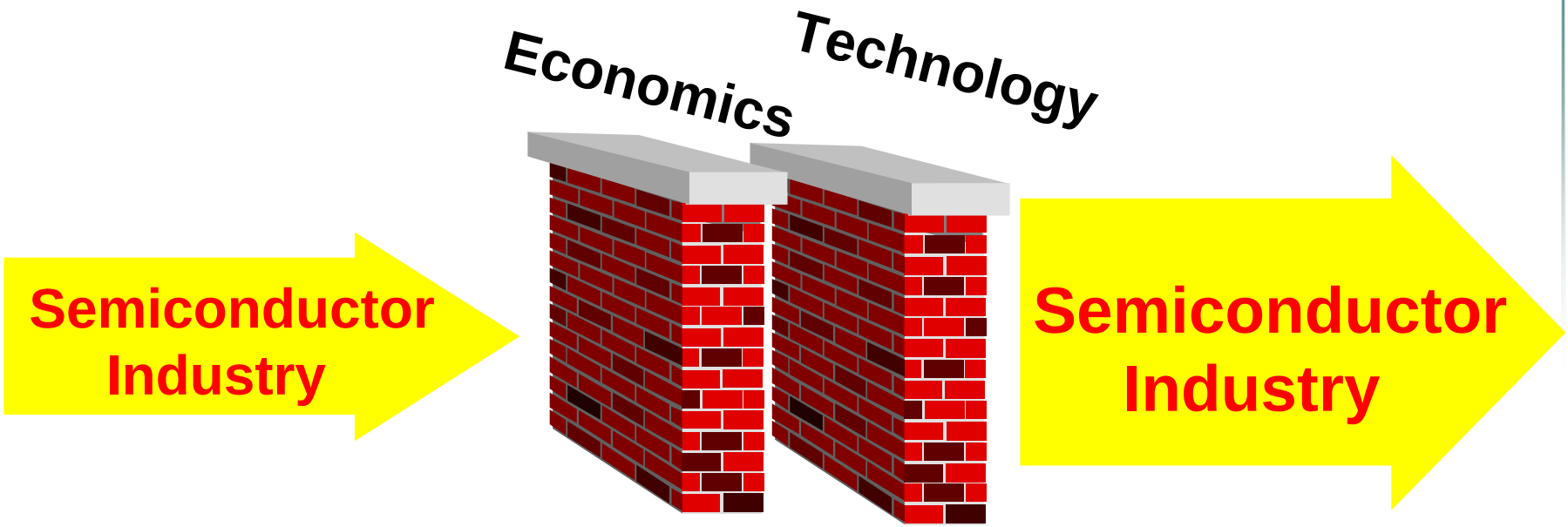
IC Makers

OEM

Implementation

The Need for Globalization

90's	21st Century



NTRS* Roadmap Editions

USA Only

1991
Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

Industry

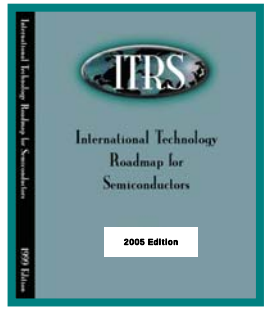
Academia

Government

*National Technology Roadmap
for Semiconductors

Roadmap Editions / Globalization

[http://public.itrs.net]



Europe

Japan

Korea

Taiwan

USA

1991
Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

1998ITRS
Update

1999ITRS

2000ITRS
Update

2001ITRS

2002ITRS
Update

2003ITRS

2004ITRS
ate

2005ITRS

Planning for Globalization - ITRS Working Groups

International Technology Working Groups (ITWG)

International Crosscut Technology Working Group (ICCT WG)

	Environment Safety & Health	Metrology	Yield Enhancement	Modeling & Simulation
System Drivers (new)				
Design				
Test				
Process Integration				
RF and Analog Mixed Signal (new)				
Emerging Research Devices & Mat'ls (new)				
Front End Processes				
Lithography				
Interconnect				
Assembly & Packaging				
Factory Integration				

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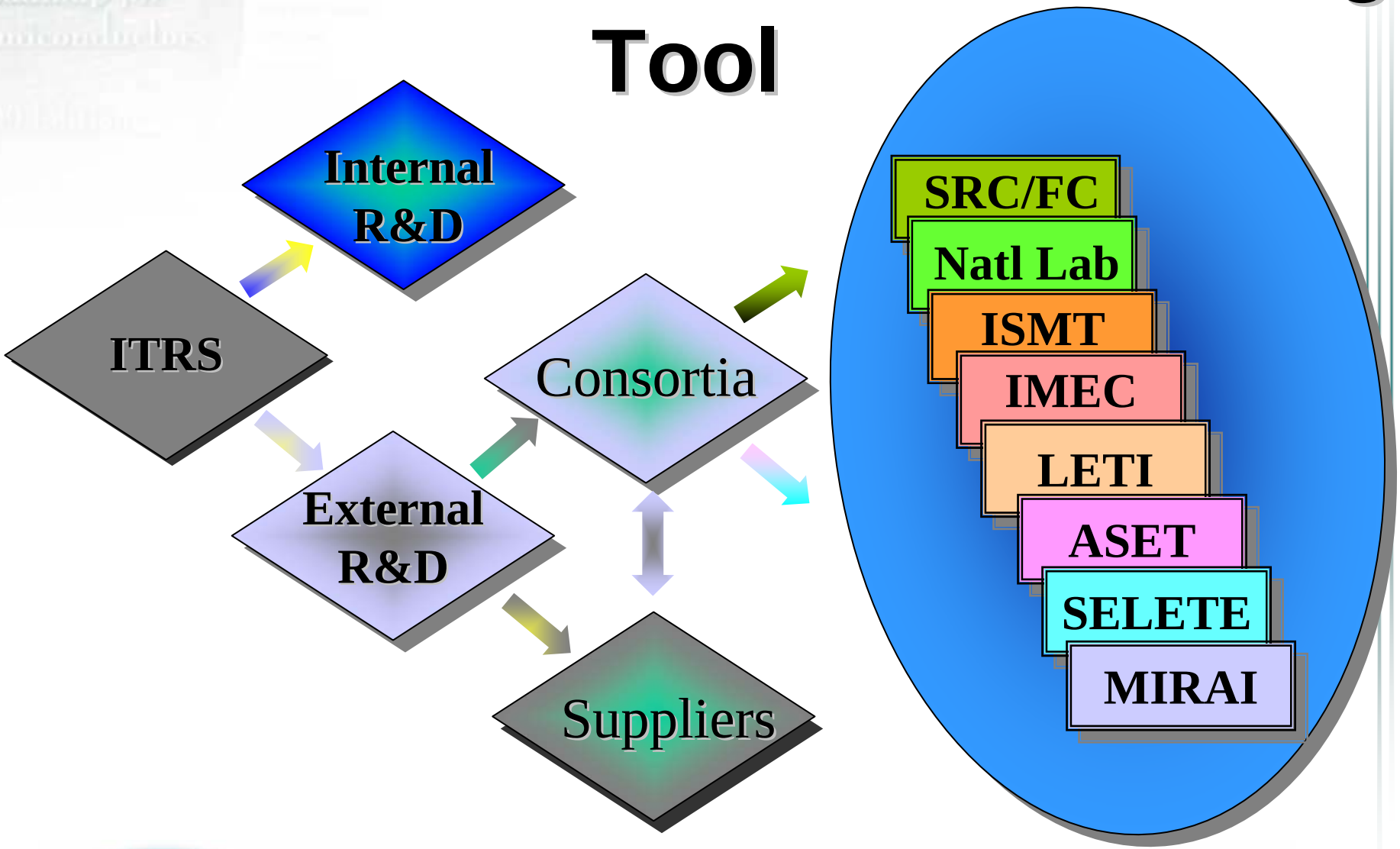
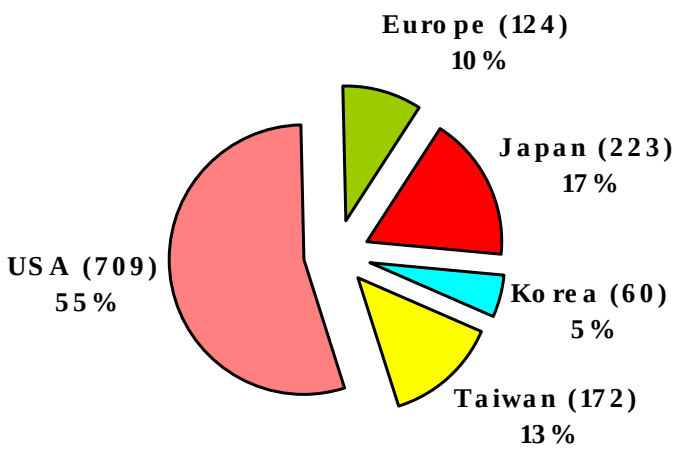
Use of ITRS as a Global Planning Tool

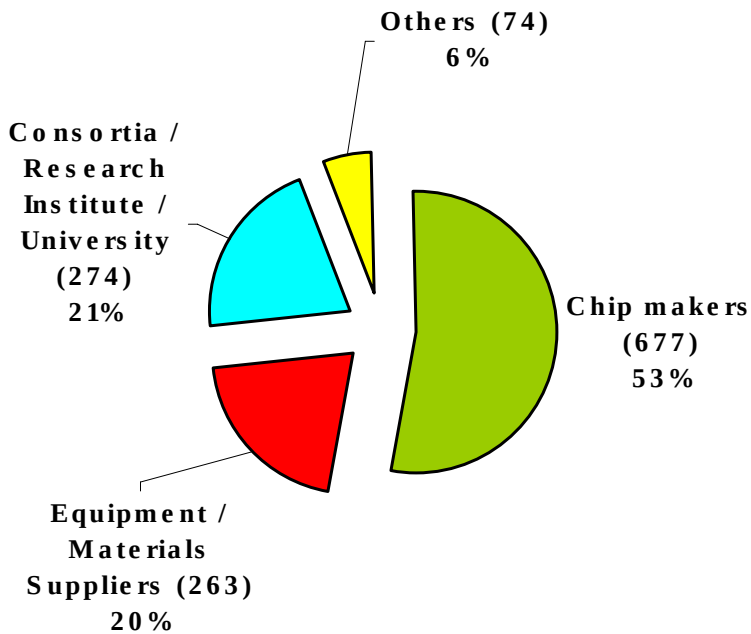


ITRS Global Demographics

2005 ITRS Members by Region



2005 ITRS Members by Affiliation



ITRS Drivers

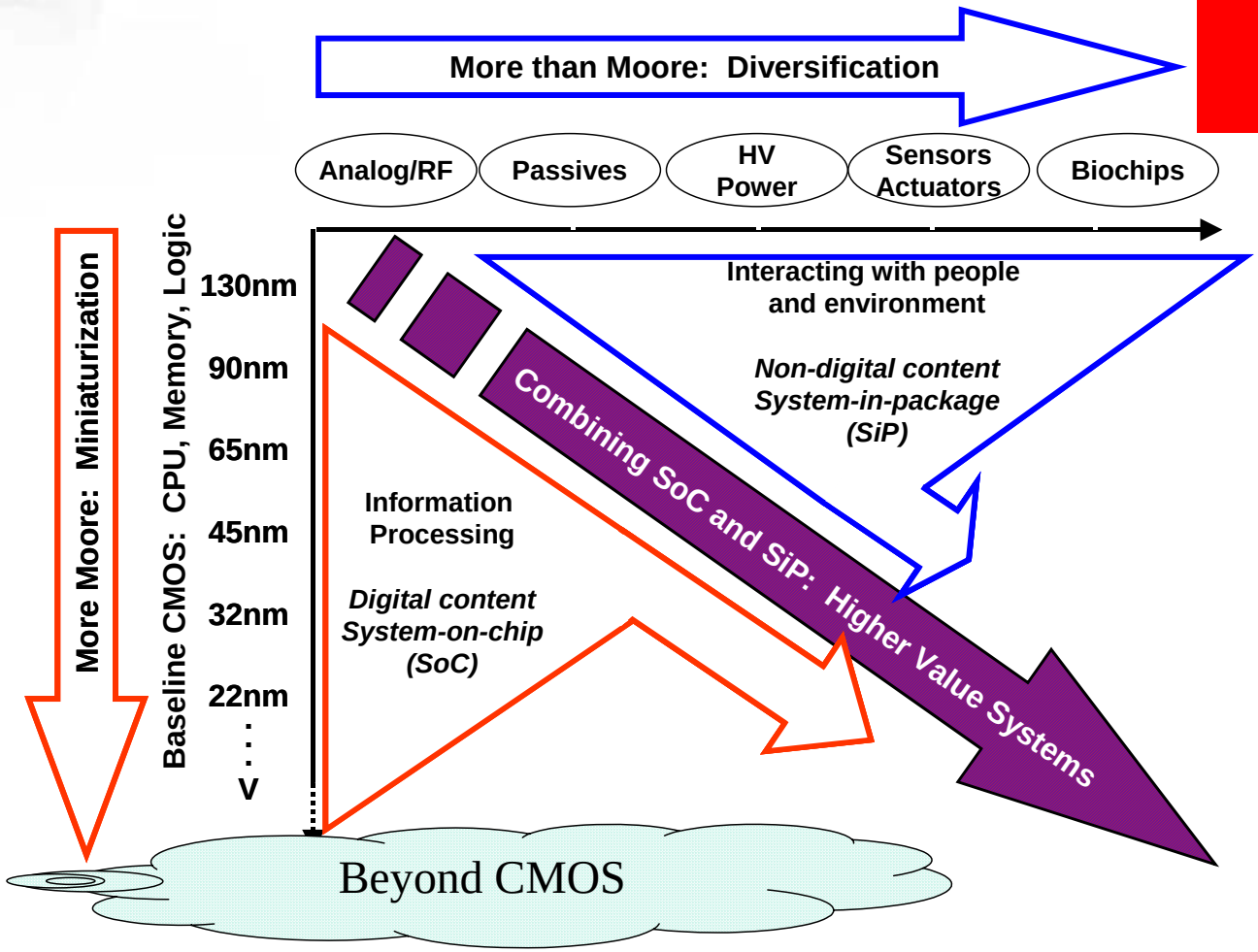
Table A Improvement Trends for ICs ***Enabled by Feature Scaling***

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

Source: 2005 ITRS, Executive Summary

Semiconductor Roadmap Driver – Scaling & Integration

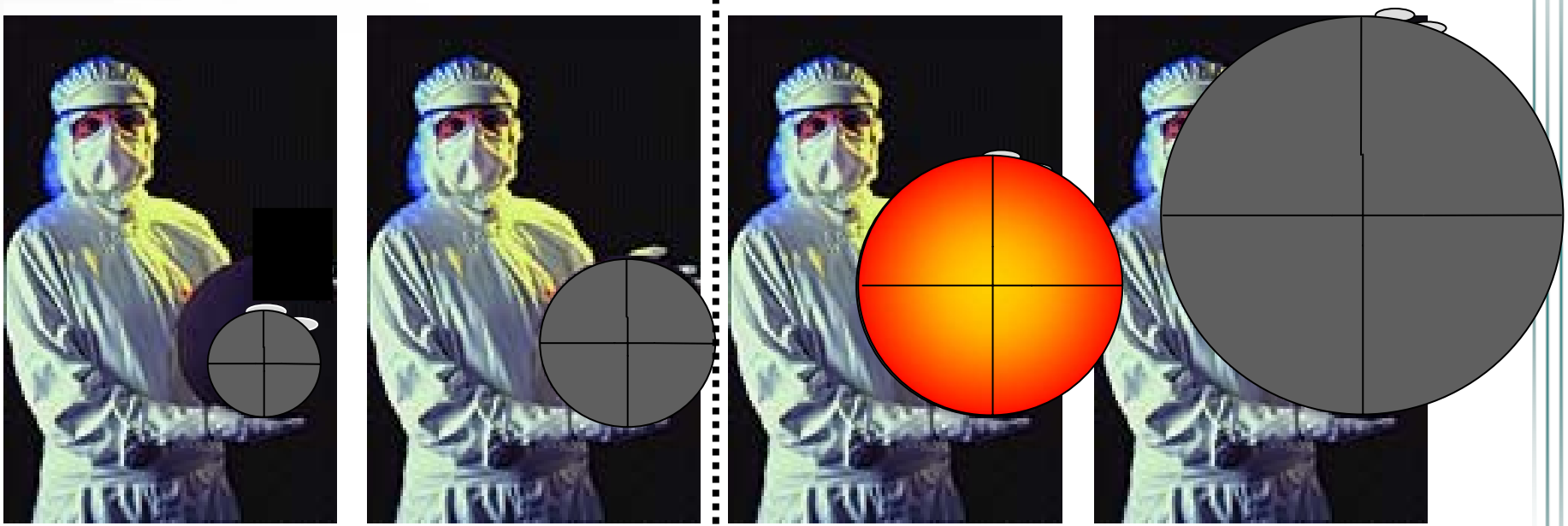
Moore's Law & More



Long Range Industry Roadmap Productivity Drivers :

Wafer Size and Technology Conversion History / Forecast

Past ← → Future



200mm/1990a | 300mm/2001a | 450mm/2012f | 675mm/2021f?

(125/150mm - 1981)

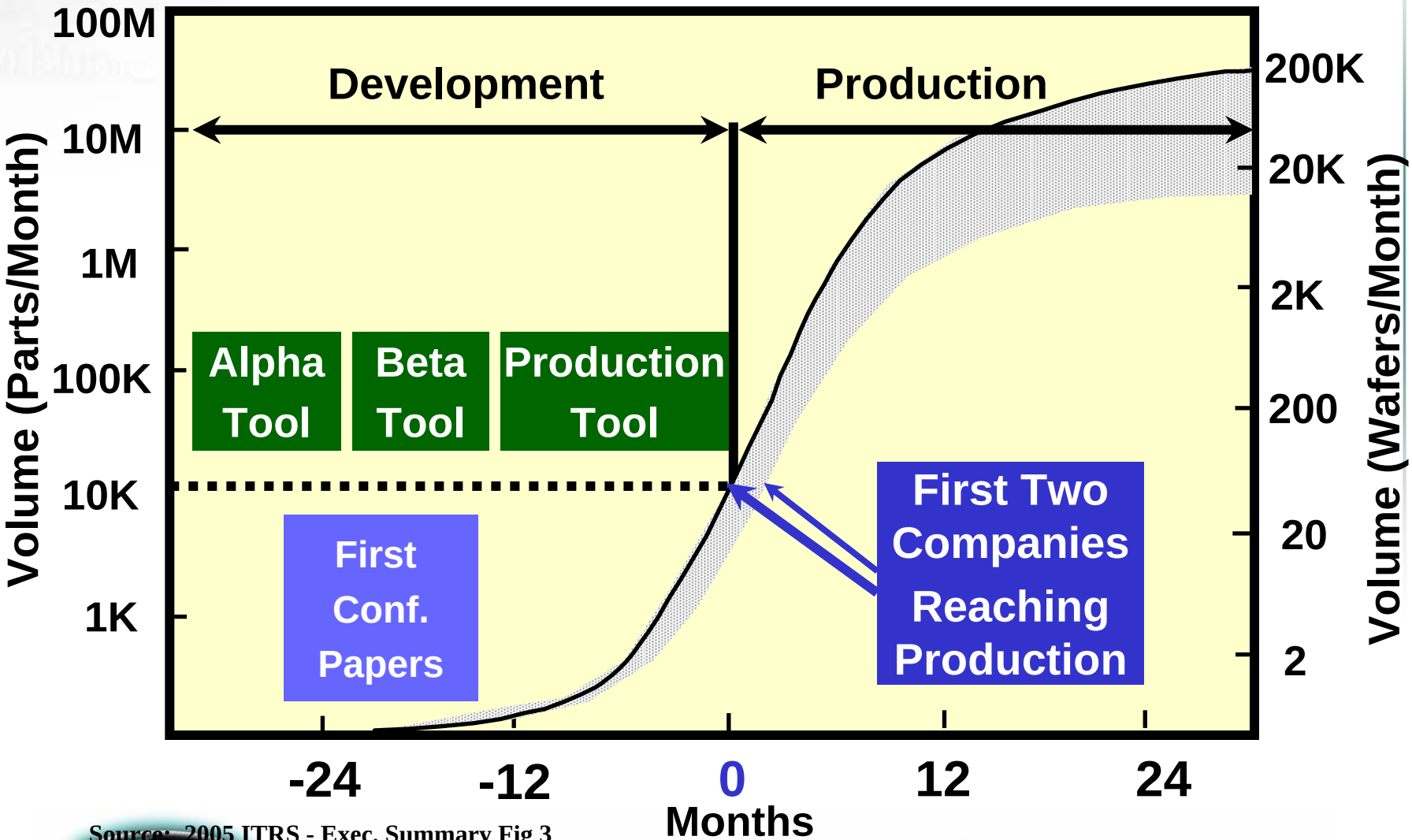
9 yrs | 9 yrs + 2yrs delay | 9 yrs + 2yrs delay | 9 yrs + 0?yrs delay | [: Wafer Scaling Cycle]

← 3-yr Cycle pace < '98a → ← 2-yr Cycle pace '98a-'04a → ← 3-yr Cycle pace > '05f – '20f → [: Technology Scaling Cycle]

Fig 3

Production Ramp-up Model and Technology

Cycle Timing



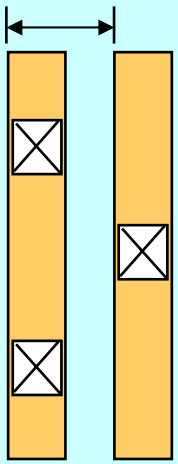
Source: 2005 ITRS - Exec. Summary Fig 3

2005 Definition of the Half Pitch

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal

Pitch

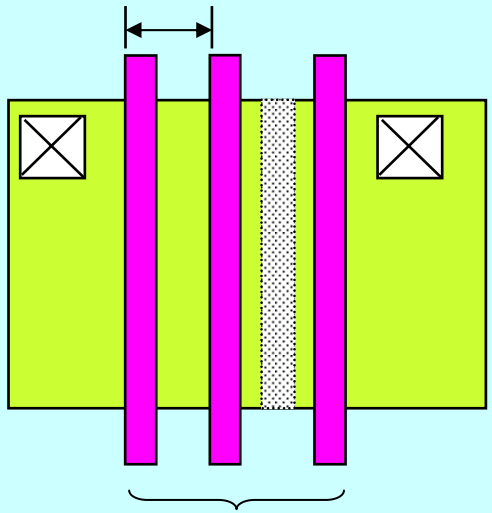


Typical DRAM/MPU/ASIC
Metal Bit Line

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

Poly

Pitch



Typical flash
Un-contacted Poly

IS: 2005 ('05-'20) ITRS Technology Trends DRAM M1 Half-Pitch : 3-year cycle

Year of Production	2000 [Actual]	2001	2002 [Actual]	2003	2004	2005	2006	2007	2008	2009	2010	2012	2013	2015	2016	2018	2019	2020
Technology - Contacted M1 H-P (nm)	180	151	130	107	90	80	71	65	57	50	45		32		22		16	14

2-Year Technology Cycle ['98-'04]

3-Year Technology Cycle

2005 ITRS Flash Poly Half-Pitch Technology: 2.0-year cycle until 1yr ahead of DRAM @65nm/'06

Year of Production	2000 [Actual]	2001	2002 [Actual]	2003	2004	2005	2006		2008	2009	2010	2012	2013	2015	2016	2018	2019	2020
Technology - Uncontacted Poly H-P (nm)	180	151	130	107	90	76	65	57	50	45		32		22		16		13

2-Year Technology Cycle ['98-'06]

3-Year Technology Cycle

2005 ITRS MPU M1 Half-Pitch Technology: 2.5-year cycle; then equal DRAM @45nm/2010

Year of Production	2000	2001	2002 [July 02]	2003	2004	2005	2006	2007 [July 08]	2008	2009	2010	2012	2013	2015	2016	2018	2019	2020
Technology - Contacted M1 H-P (nm)	180	157	136 [130]	119	103	90	78	68 [65]	59	52	45		32		22		16	14

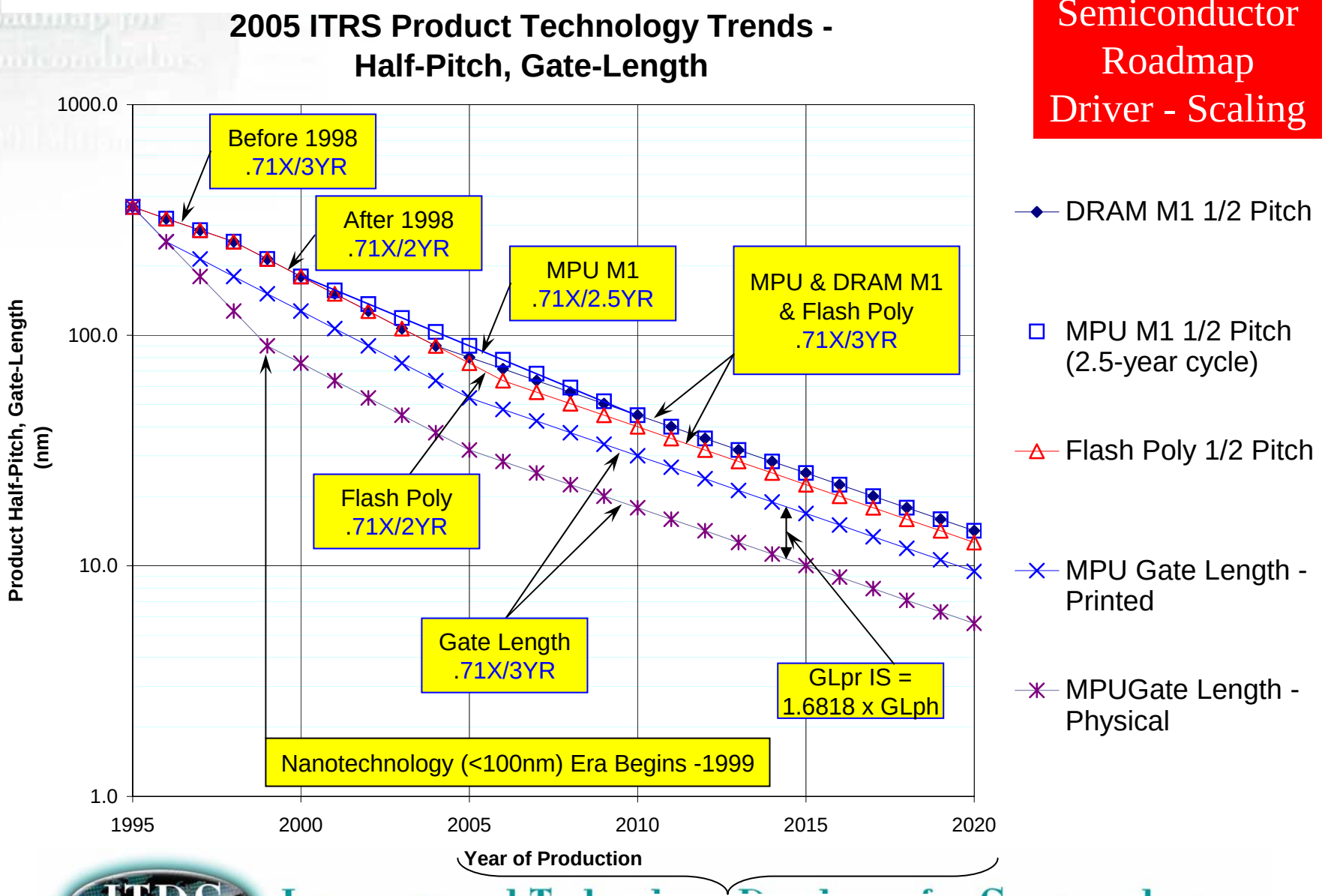
3-2-Yr Cycle]

2.5-Year Technology Cycle

3-Year Technology Cycle

Note: Faster introduction of half-poly pitch from Flash is expected; Doubling of transistors every 2 years from MPU/ASIC is expected

Figure 8 ITRS Product Technology Trends

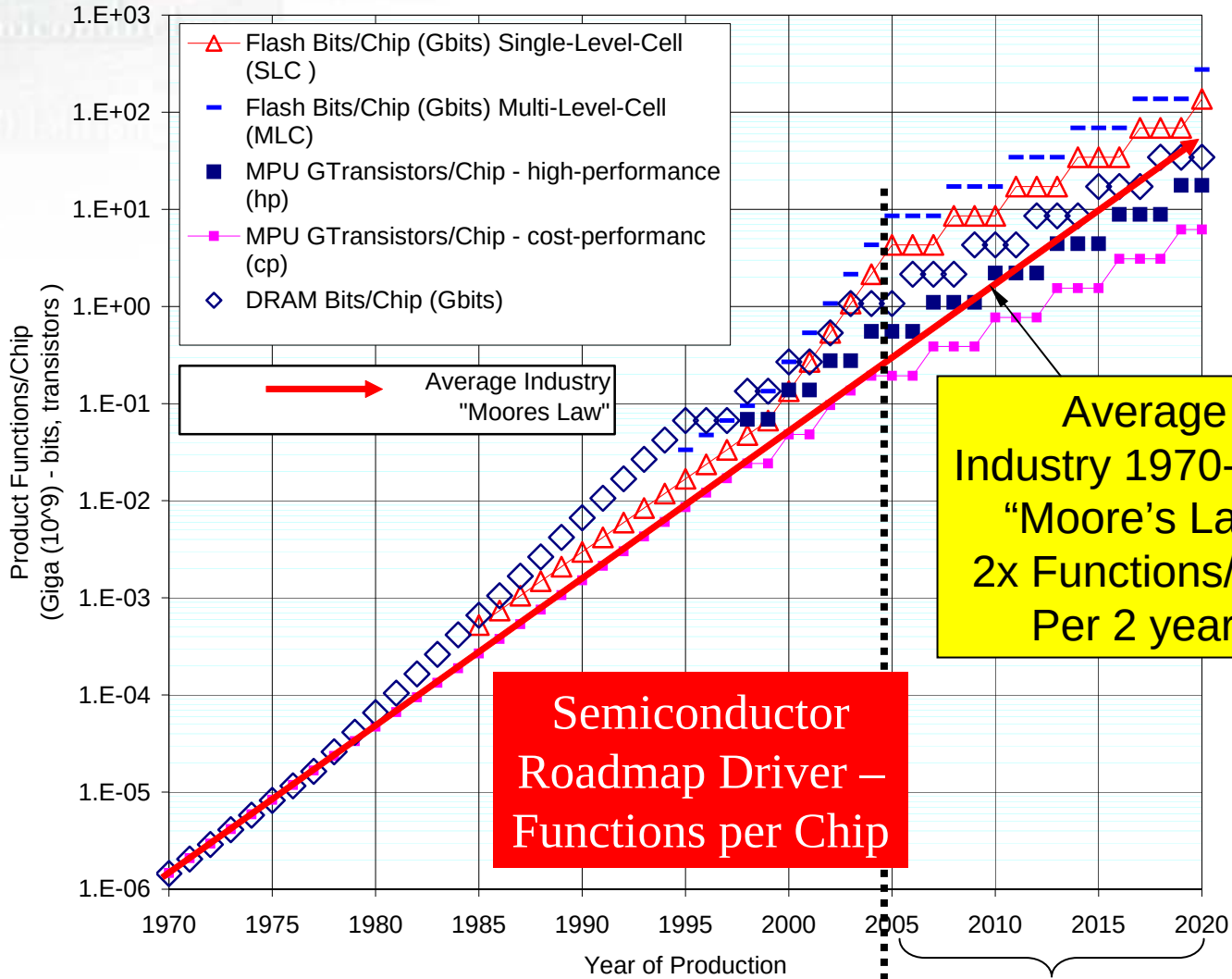


Source: 2005 ITRS – Exec. Summary/ORTC Fig 8

Chip Size Trends – 2005 ITRS Functions/Chip Model IS

2005 ITRS Product Technology Trends
Functions/Chip

(@Volume Production, Affordable Chip Size**)



** Affordable Production
Chip Size Targets:
DRAM, Flash < 145mm^2
hp MPU < 310mm^2
cp MPU < 140mm^2

Average Industry 1970-2020
"Moore's Law"
2x Functions/chip
Per 2 years

MPU ahead or = "Moore's Law"
2x Xstors/chip
Per 2 years
Thru 2010

Semiconductor Roadmap Driver – Functions per Chip

** Example
Chip Size Targets:
1.1Gt P07h MPU
@ intro in 2004/620mm^2
@ prod in 2007/310mm^2

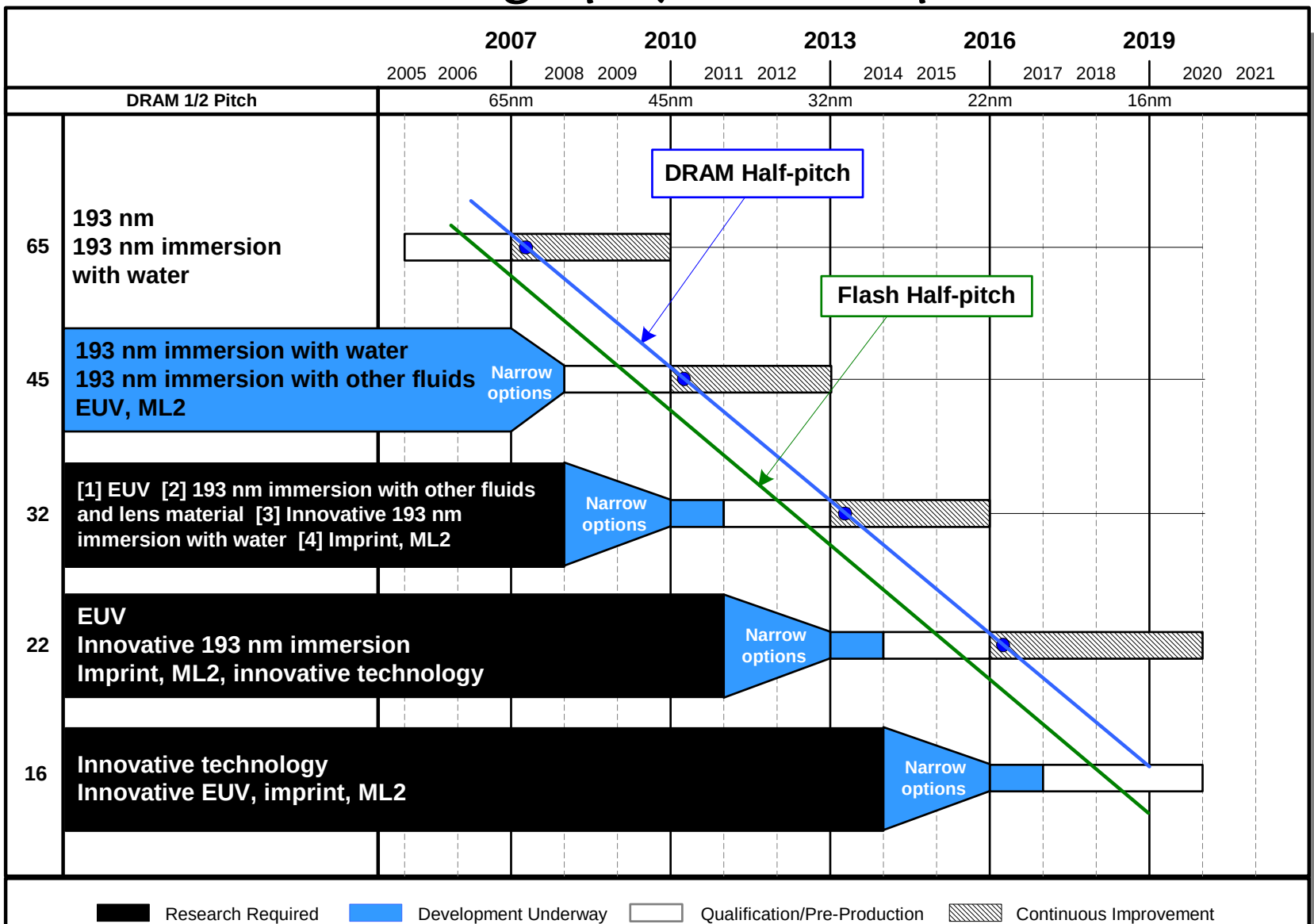
** Example
Chip Size Targets:
0.39Gt P07c MPU
@ intro in 2004/280mm^2
@ prod in 2007/140mm^2

Past ← → Future

Changes of Lithography Potential Solutions in 2005

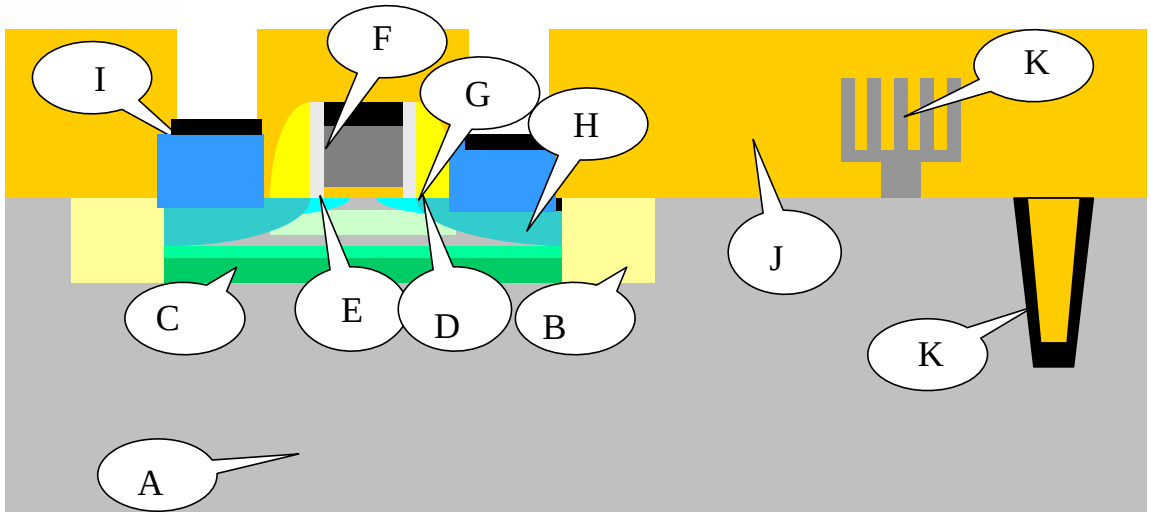
- 193nm immersion with water and other fluids expected to be primary technology through 45nm and perhaps 32nm ½ pitch with new lens materials
- 157nm no longer anticipated as potential solution
- EUV remains most likely next generation lithography (NGL) with possible use starting at 45nm ½ pitch and primary solution for 32nm and 22nm ½ pitch
- Electron projection and proximity electron no longer anticipated as potential solutions
- Imprint extended to cover 32nm through 16nm ½ pitch
- Maskless lithography remains as potential solution starting at 45nm ½ pitch

Lithography Roadmap



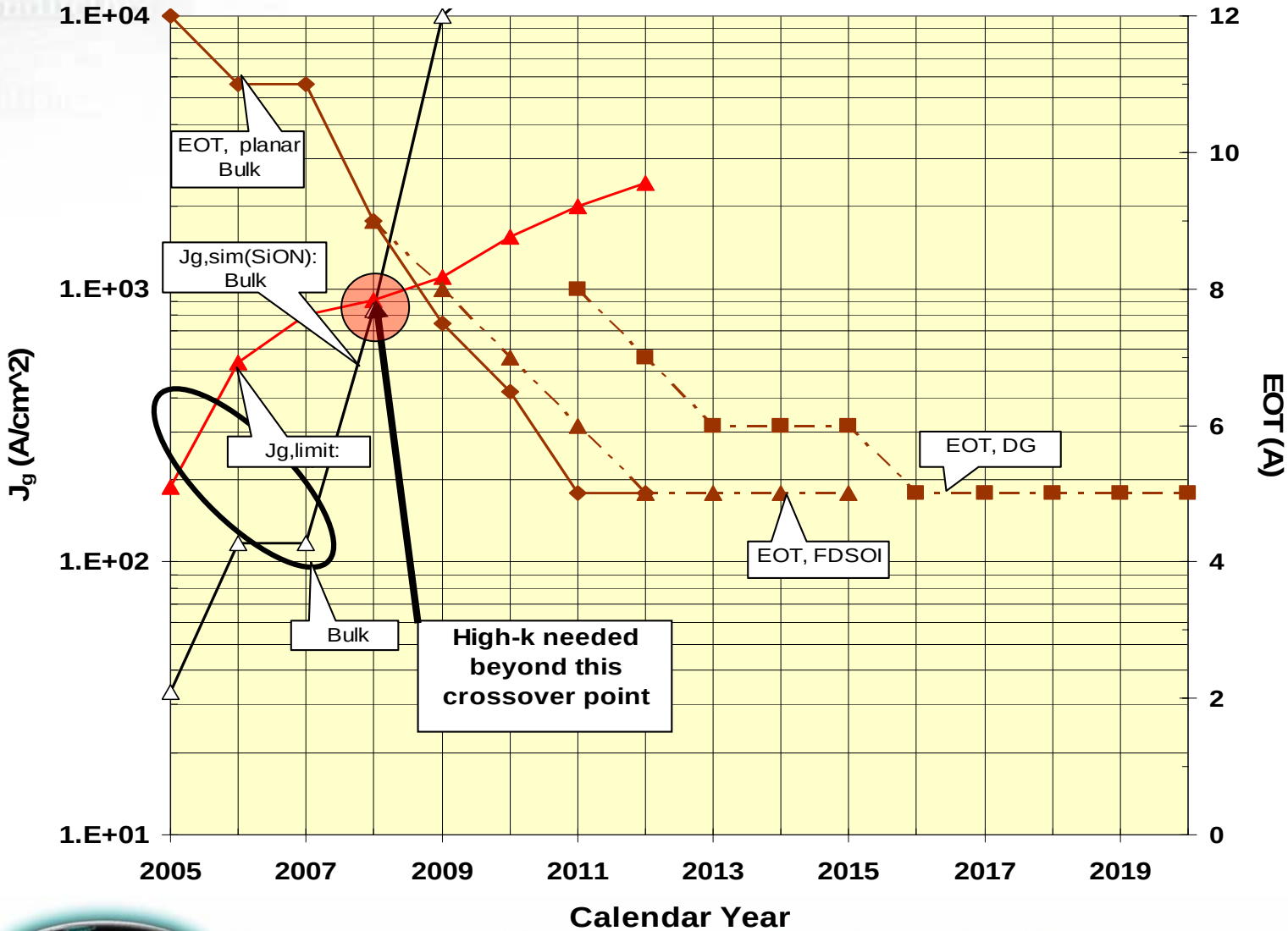
This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Transistor Challenges



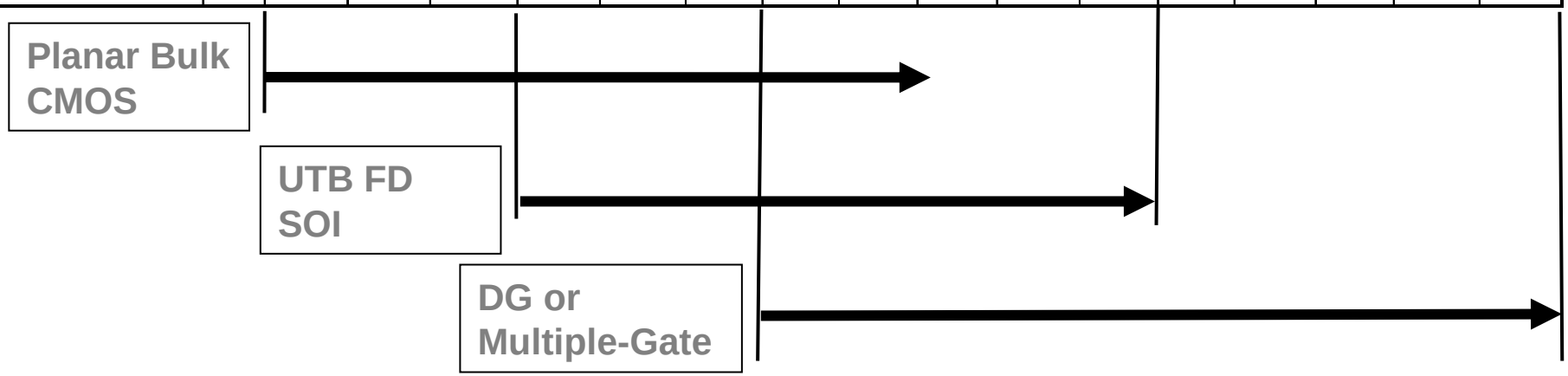
A: Starting Material
B: Isolation
C: Well Doping
D: Channel Surface (Preparation)
E: Channel Doping and Channel Strain
F: Gate Stack (Including Flash) and Spacer
G: Extension Junction and Halo
H: Contacting Source/Drain Junction
I: Elevated Junction and Contacts
J: Premetal Dielectric
K: DRAM Stack/Trench Capacitor & FeRAM Storage

Transistor Gate High-k Materials after 2008



Multiple Parallel Paths for High-Performance Logic in 2005 ITRS

Year in Production		2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Physical Lgate (High Performance)	nm	32	28	25	22	20	18	16	14	13	11	10	9	8	7	6	5

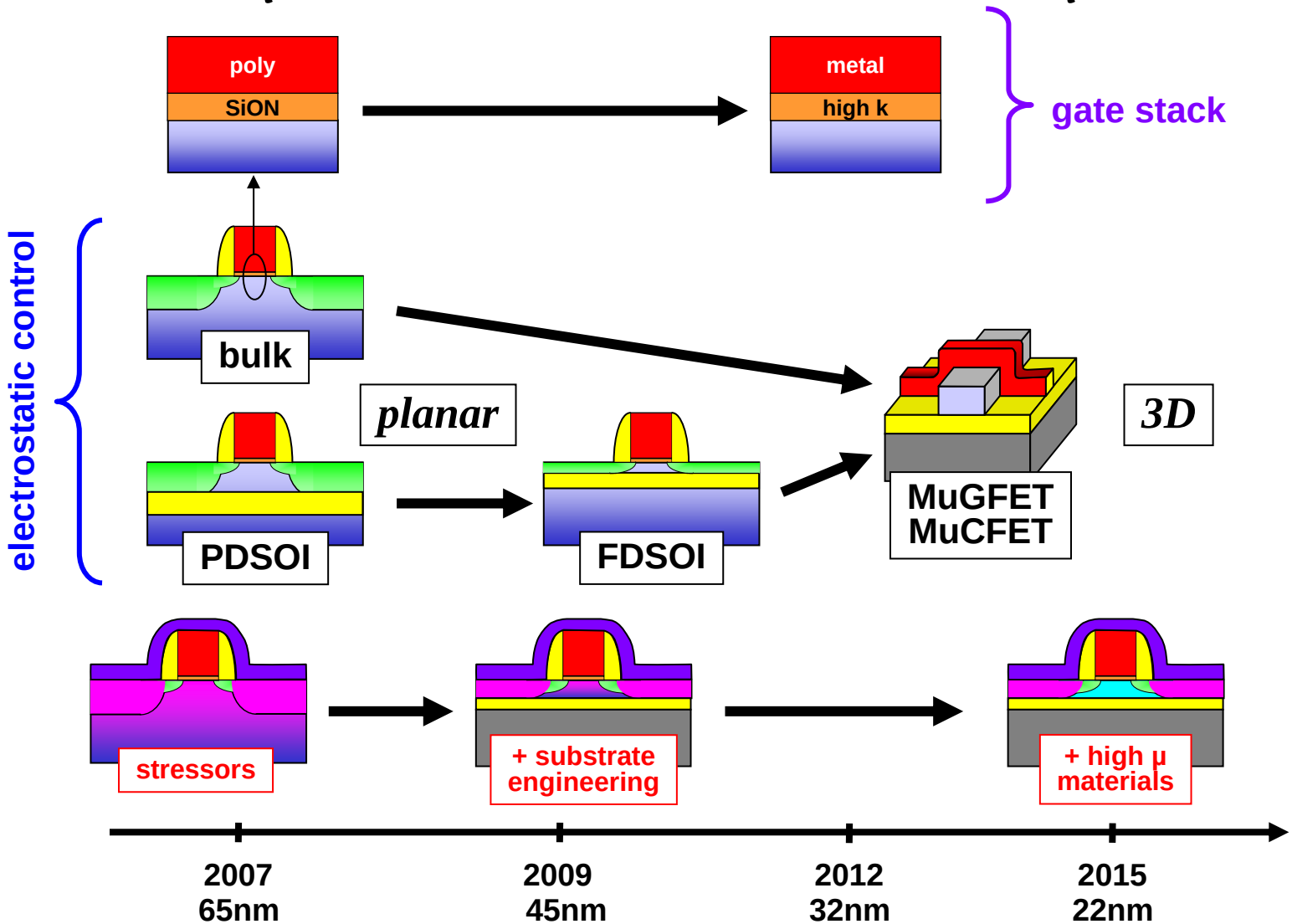


Multiple parallel paths reflects most likely scenario:

- **Some companies will extend planar bulk CMOS as long as possible**
- **Others will switch to FDSOI and/or multiple gate earlier**
- **Ultimate MOSFET is multiple gate**
- **Similar multiple paths for low-power logic**

Preliminary Results

Simplified Transistor Roadmap

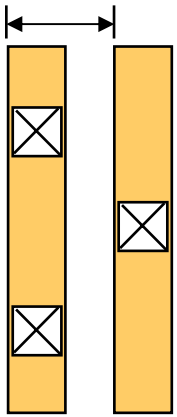


Source: European Nanoelectronics Initiative Advisory Council (ENIAC)

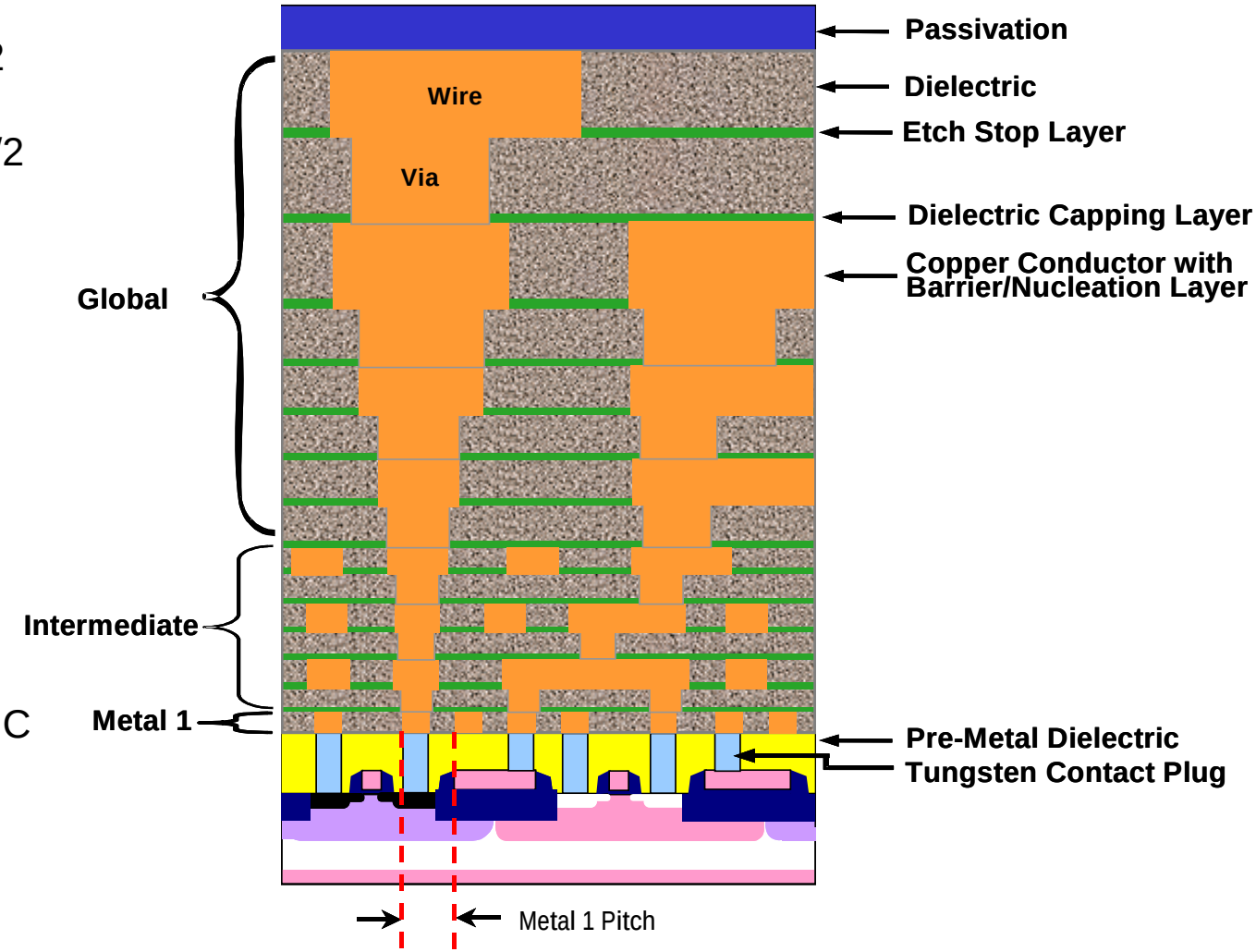
Typical Interconnect Stack

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

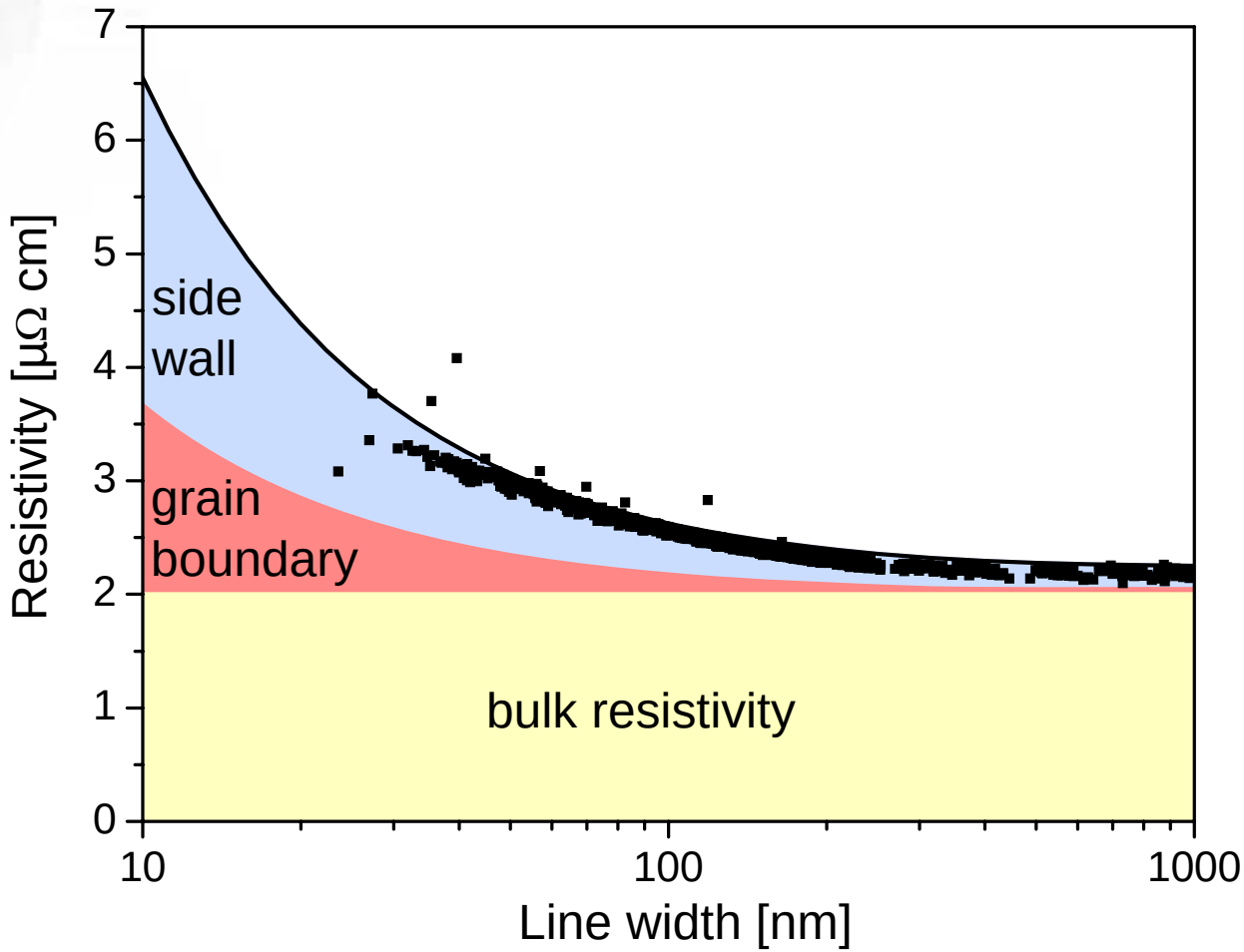
Metal Pitch



Typical DRAM/MPU/ASIC
Metal Bit Line



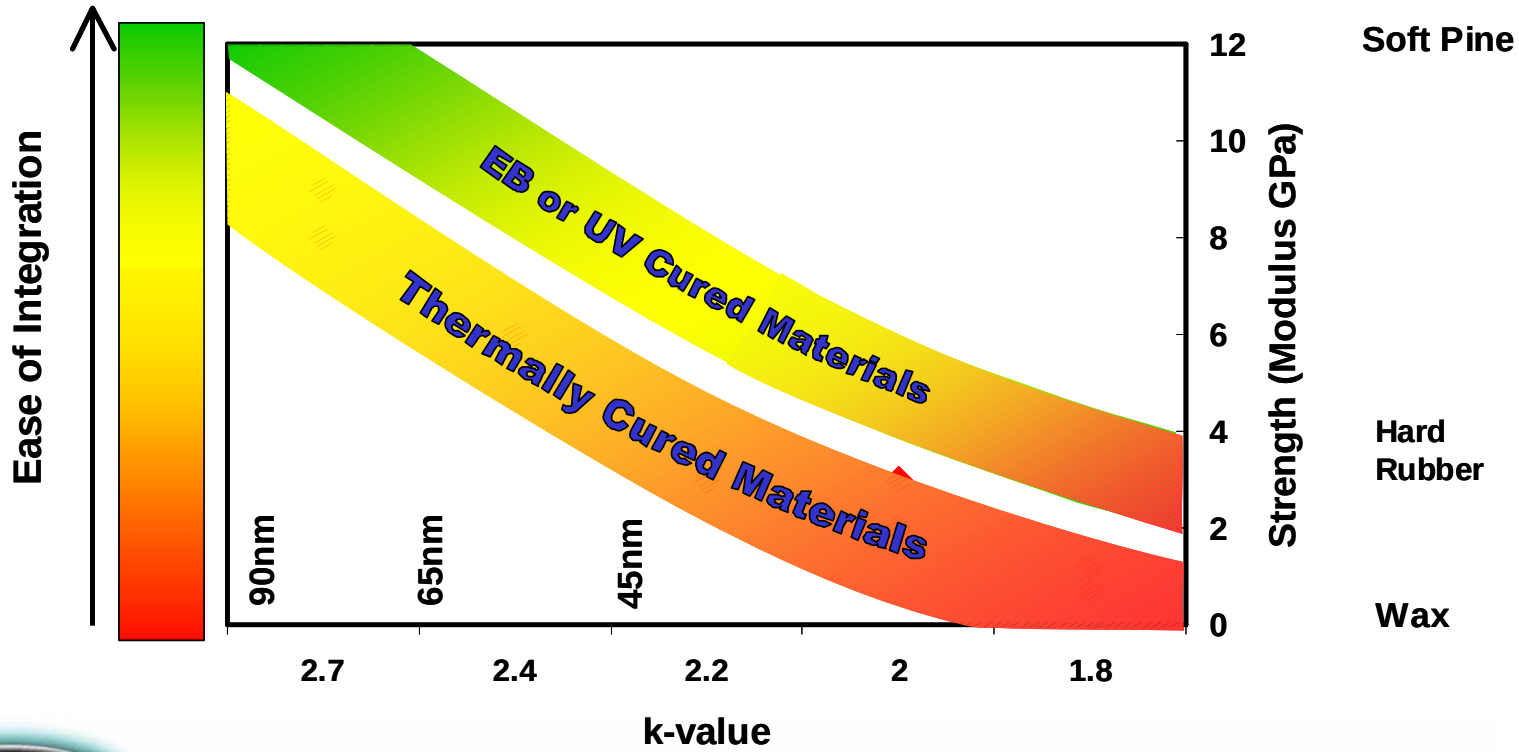
Challenges in Scaling Conductors

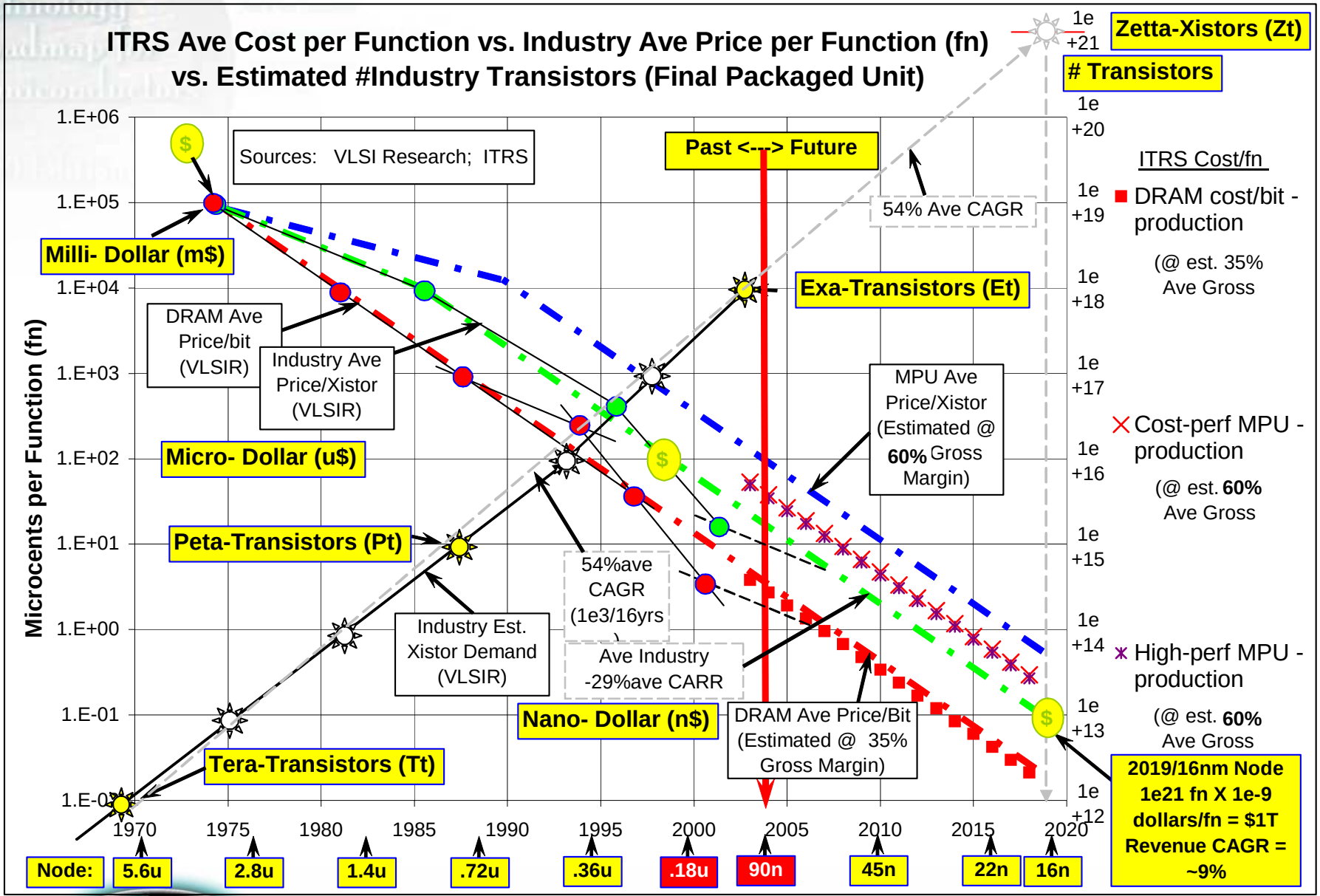


Source: Infineon Technologies

Challenges in Scaling Inter-Metal Dielectrics

- Low k materials with k~2.7 are in manufacturing and materials with k~2.4 will be developed in 2~3 years.
- Securing mechanical properties of the Ultra Low k materials is a challenge.

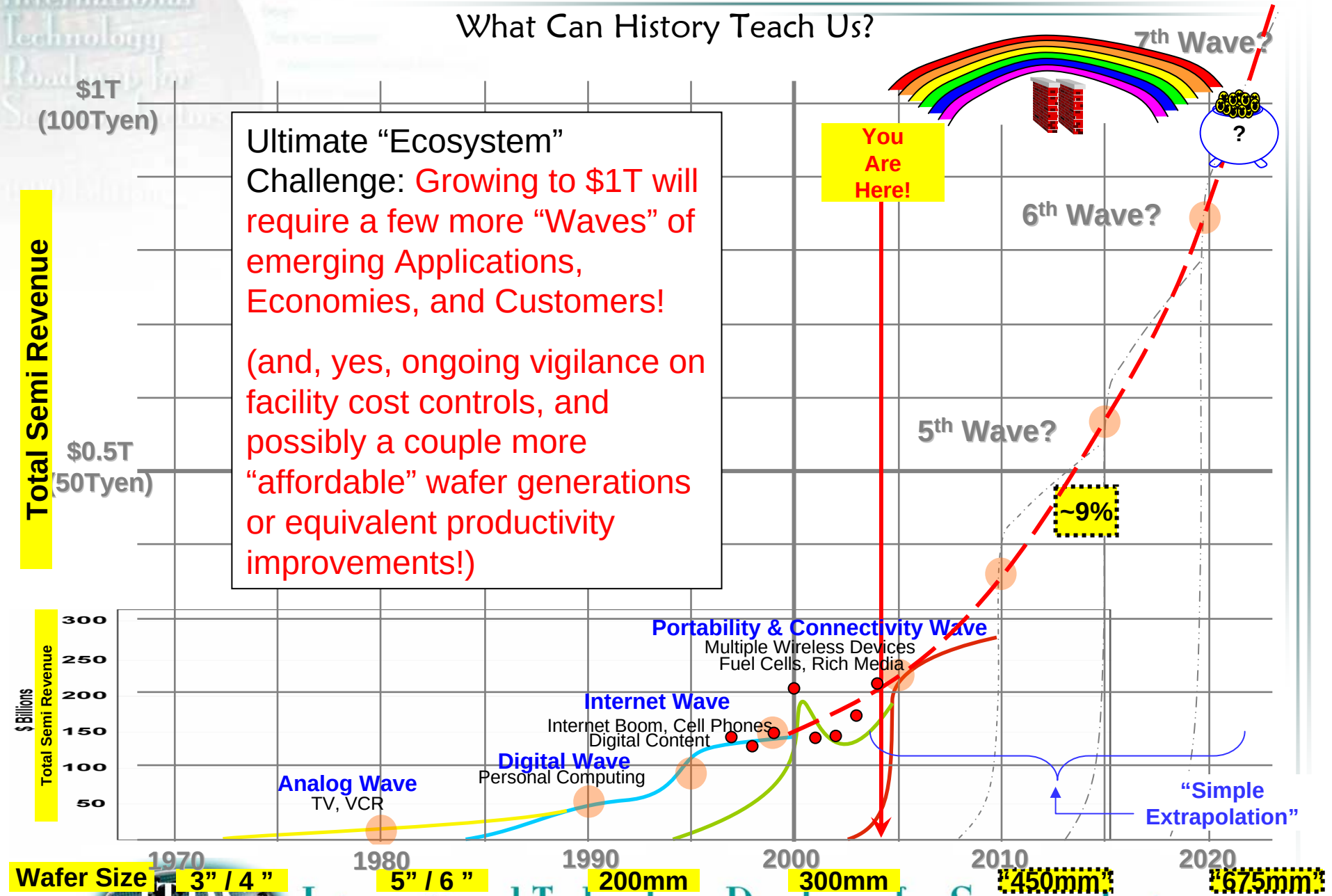




International Technology Roadmap for Semiconductors

Sources: ITRS; VLSIR [+ "Simple Extrapolation"]

What Can History Teach Us?



Source: Semico Research Corp, May'04 [+ "Simple Extrapolation"]

Key Messages for 2005

- Global Roadmap consensus building and R&D support has become a necessity to plan and guide R&D solutions to industry grand challenges.
- Lithography is not a limiter down to 45nm. Exposure tools with 193nm wavelength will dominate the next technology generations (65nm, 45nm and may be 32/22nm) with both dry and immersion solutions.
- EUV will challenge 193nm at 32/22nm.
- Control of critical dimension (CD) below 4nm was identified as a major issue.
- Introduction of 450mm wafers in the 2012 timeframe.
- Mobility enhancement techniques will enable increased transistor performance without the introduction of high-k gates and metal electrodes materials for 65nm and may be for 45nm.
- Low-k roadmap essentially unchanged for the first time in 10 years. Materials with k~2.7 are in manufacturing and k~2.4 materials will follow.
- Many new package solutions required to increase functionality and to reduce cost will require additional attention in the future.
- Industry Economic outlook could be very good, even under slower growth scenario, as long as demand remains strong and productivity and performance goals are achieved.

For detailed 2005 ITRS Tables and Text, Visit Online at:

http://public.itrs.net

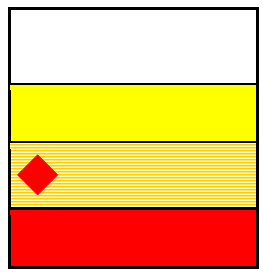
When you visit, Note: ITRS Table Colorization Code Reference:

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



ITRS Backup 1

- 2005 Executive Summary Roadmap

The International Technology Roadmap for Semiconductors (ITRS) is the result of a worldwide consensus-building process. This document predicts the main trends in the semiconductor industry spanning across 15 years into the future. The participation of experts from Europe, Japan, Korea, and Taiwan as well as the U.S.A. ensures that the ITRS is a valid source of guidance for the semiconductor industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. These five regions jointly sponsor the ITRS.

The Semiconductor Industry Association (SIA) coordinated the first efforts of producing what was originally *The National Technology Roadmap for Semiconductors* (*NTRS*). The semiconductor industry became a global industry in the 1990s, as many semiconductor chip manufacturers established manufacturing or assembly facilities in multiple regions of the world. This realization led to the creation of the *International Technology Roadmap for Semiconductors* in the late 90s. The invitation to cooperate on the ITRS was extended by the SIA at the World Semiconductor Council in April 1998 to Europe, Japan, Korea, and Taiwan. Since then, full revisions of the ITRS were produced in 1999, 2001 and 2003; ITRS updates were produced in the even-numbered years (2000, 2002, 2004).

The 2005 ITRS represents a major departure from the previous versions of Roadmaps because it removes the concept of "technology node" as the main pace setter for the IC industry. In the past, DRAM products set the technology pace by quadrupling the number of bits every three years with the introduction of a new major technology generation. The relation among transistor density (4×) and metal half-pitch (×0.7) and year of introduction (three-year) remained constant from the mid-70s to the mid-90s. The reduction from generation to generation of the DRAM half-pitch of metal by 30% (0.7× the previous technology generation) identified a "technology node." However, the increase in the number of bits by four times from one technology node to the next led to a continuous increase in die size that eventually negatively affected the economics of this silicon cycle. In an attempt to minimize the increase in die size many IC companies accelerated the speed at which new technology nodes were introduced from a three-year cycle to a 2–2 ½-year cycle in the second half of the 90s.

As device features become smaller, MPU and Flash technologies have been approaching (and in some cases producing) features even smaller than DRAM. Additionally, MPU and Flash products have been introduced at a comparable or, at times, even faster pace than DRAMs. As a result, the use of a single number (such as a technology node) derived from the half-pitch of DRAM no longer suffices to characterize the whole semiconductor industry. The 2005 ITRS addresses an independent measure of the technology pace of DRAM, of MPU, and of Flash products.

Another change in the 2005 ITRS indicates the growing interest in new nanoscale devices representing alternatives to CMOS. Emerging Research Devices topics are now addressed in a separate chapter from the Process Integration, Devices, and Structures chapter. Indeed, even though CMOS is (and will remain) the industry workhorse up to and beyond the year 2020, it is anticipated that new devices will be introduced in the latter half of the next decade utilizing different and new ways of processing and storing information. Most of the proposed devices rely very heavily on new material properties and therefore, a new sub-chapter on Emerging Research Materials has been added to the ERD chapter.

In conclusion, it is the purpose of the ITRS documents to provide a reference of requirements, potential solutions, and their timing for the semiconductor industry. This objective has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university, consortia, and government labs.

The ITRS documents have become and remain a truly common reference for the entire semiconductor industry. Indeed, the cooperative efforts of the ITRS participants have fostered cooperation among international consortia, universities, and research institutions around the world. It is hoped that the 2005 ITRS will further contribute to stimulate cooperative R&D investments so that the financial burden can be more uniformly shared by the whole industry. It is also hoped that the 2005 ITRS will continue to stimulate the fundamental elements that encourage innovation in individual companies.

Litho Table 3a - Equip (Near Term) (Draft review 10/21/05):

Table 3a Lithography Technology Requirements—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
DRAM and Flash									
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	36	32
Flash ½ pitch (nm) (un-contacted poly)	76	64	57	51	45	40	36	32	28
Contact in resist (nm)	94	79	70	63	56	50	44	39	35
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Overlay [A] (3 sigma) (nm)	15	13	11	10	9	8	7.1	6.4	5.7
CD control (3 sigma) (nm) [B]	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
MPU									
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21
MPU physical gate length (nm) *	32	28	25	23	20	18	16	14	13
Contact in resist (nm)	111	97	84	73	64	56	50	44	39
Contact after etch (nm)	101	88	77	67	58	51	45	40	36
Gate CD control (3 sigma) (nm) [B] **	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
Chip size (mm^2)									
Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858	858	858
Number of mask levels MPU	33	33	33	35	35	35	35	35	35
Number of mask levels DRAM	24	24	24	24	24	26	26	26	26
Wafer size (diameter, mm)	300	300	300	300	300	300	300	450	450

* MPU physical gate length numbers are supplied by Front End Processes w... ...TC Tables 1a and 1b.

** Noted exception for RED in next three years: Solution NOT known, but d... ...turing.

"65nm" ←→ "45nm"

IEM Sc. C

International Technology Roadmap for Semiconductors

Litho Table 3b - Equip (Long Term) (Draft review 10/21/05):

Table 3b Lithography Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
DRAM and Flash							
DRAM ½ pitch (nm)	28	25	22	20	18	16	14
Flash ½ pitch (nm) (un-contacted poly)	25	23	20	18	16	14	13
Contact in resist (nm)	31	28	25	22	20	18	16
Contact after etch (nm)	28	25	23	20	18	16	14
Overlay [A] (3 sigma) (nm)	5.1	4.5	4.0	3.6	3.2	2.8	2.5
CD control (3 sigma) (nm) [B]	3.0	2.6	2.3	2.1	1.9	1.7	1.5
MPU							
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	22	20	18	16	14
MPU gate in resist (nm)	19	17	15	13	12	11	9
*MPU physical gate length (nm) **	11	10	9	8	7	6	6
Contact in resist (nm)	35	31	28	25	22	20	18
Contact after etch (nm)	32	28	25	23	20	18	16
Gate CD control (3 sigma) (nm) [B]	1.2	1.0	0.9	0.8	0.7	0.7	0.6
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	22	20	18	16	14
Chip size (mm^2)							
Maximum exposure field height (mm)	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858
Number of mask levels MPU	37	37	39	39	39	39	39
Number of mask levels DRAM	26	26	26	26	26	26	26
Wafer size (diameter, mm)	450	450	450	450	450	450	450

* MPU physical gate length numbers are supplied by Front End Processes working group and found in the ORTC Tables 1a and 1b